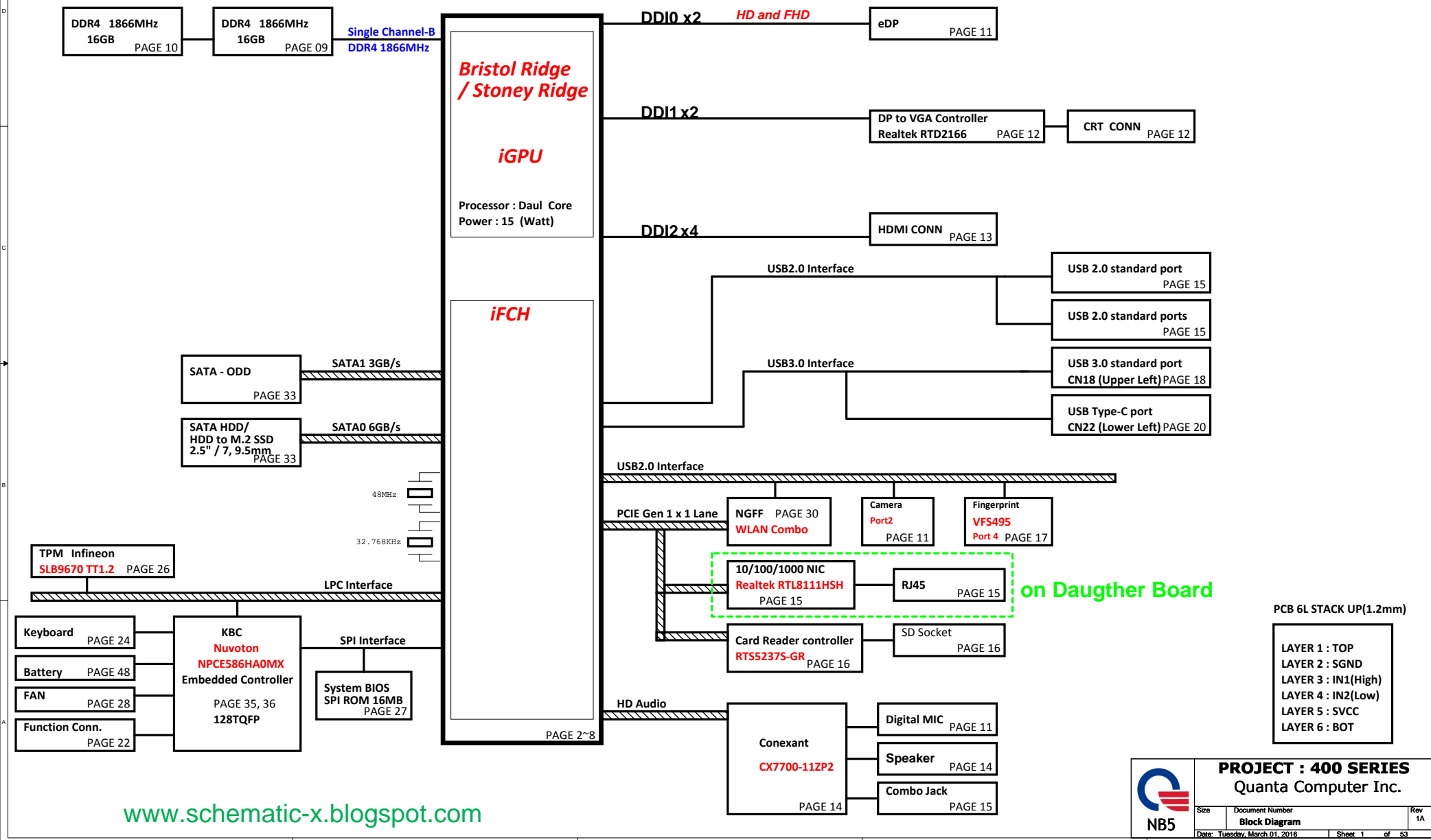
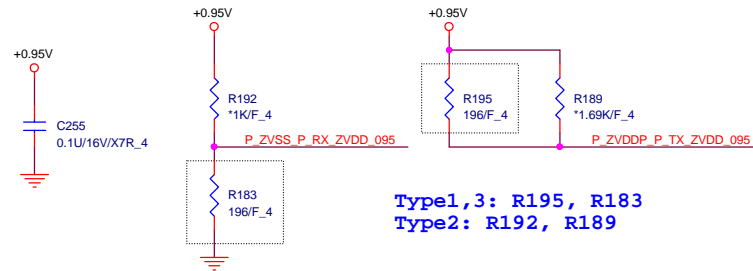
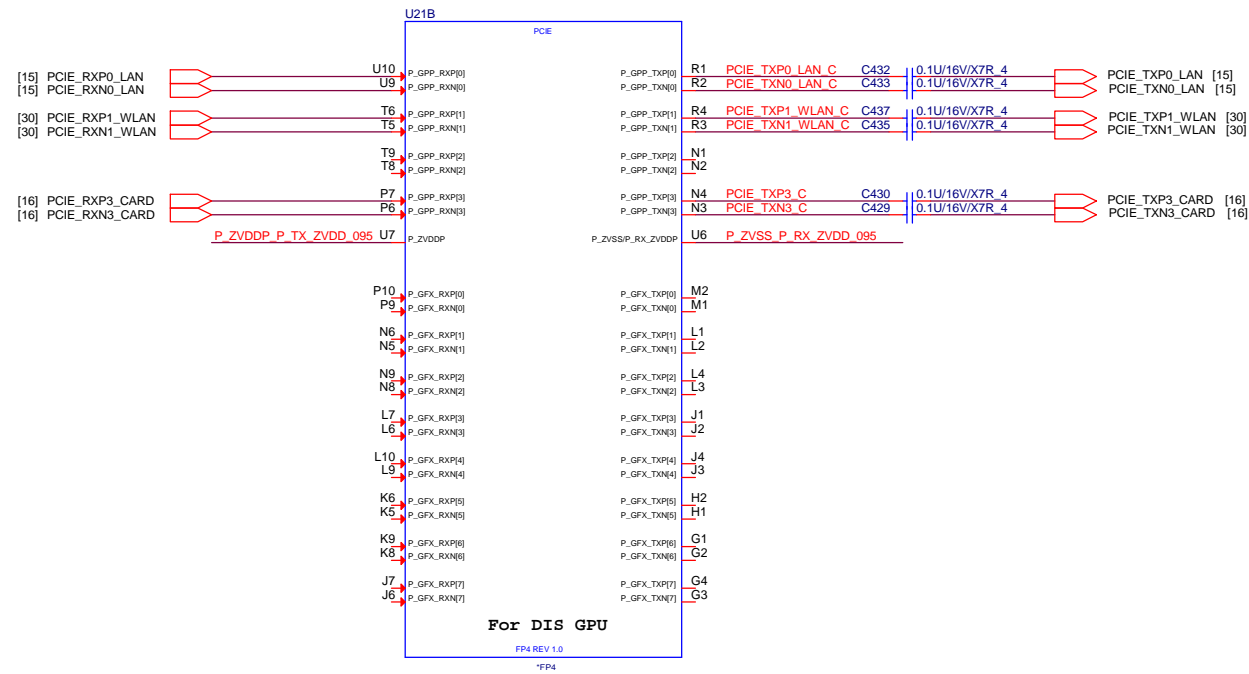


# 400 series Pitt / X93A (UMA) Schematics

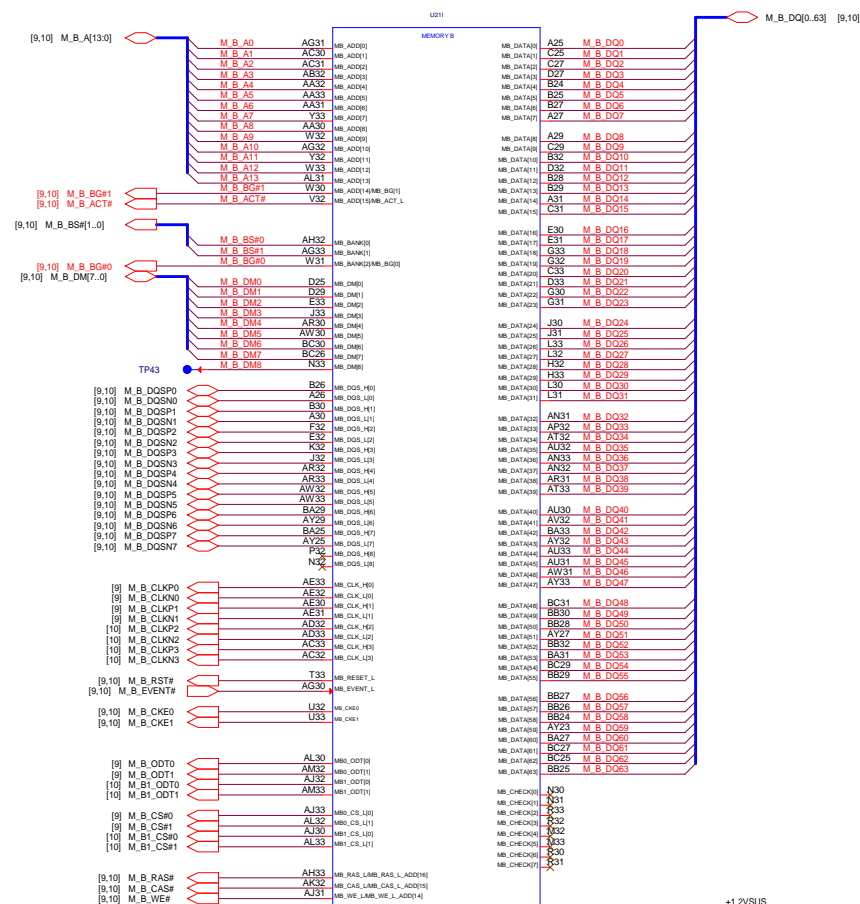
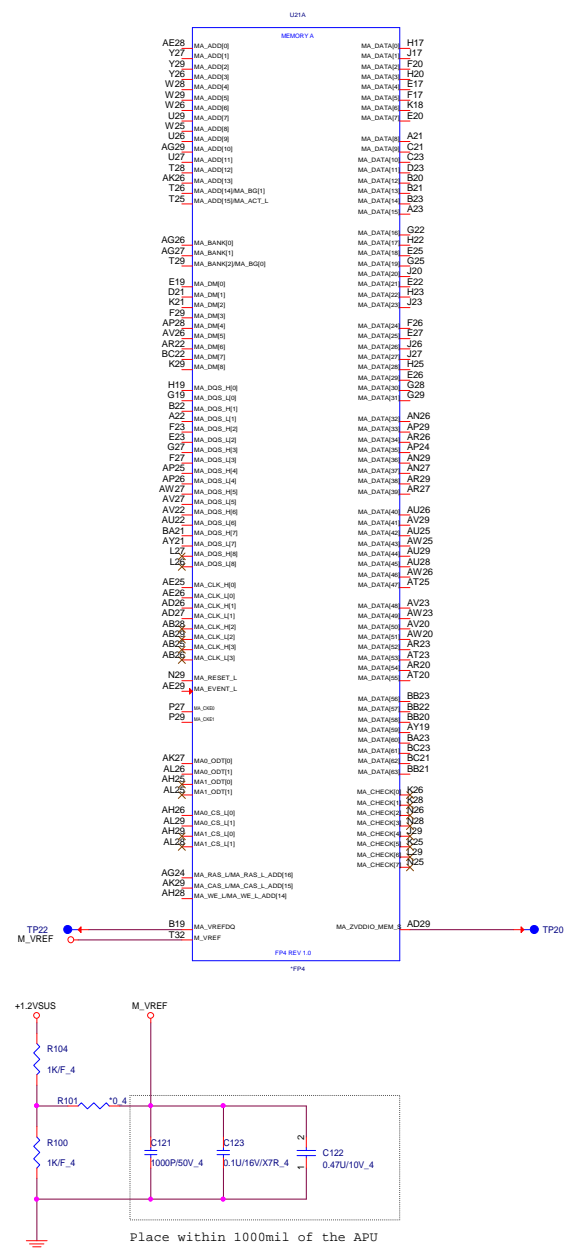
01





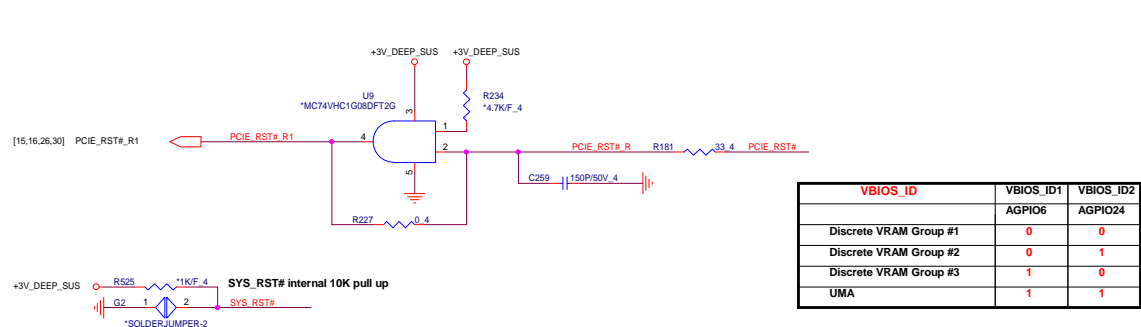
**PROJECT : 400 SERIES**  
Quanta Computer Inc.

Size	Document Number	Rev
	BR/ST 1/7 (PCIE)	1A
Date: Tuesday, March 01, 2016		Sheet 2 of 53

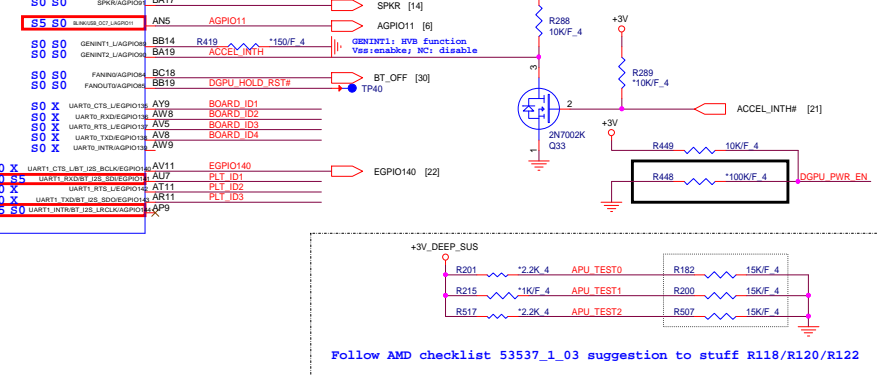
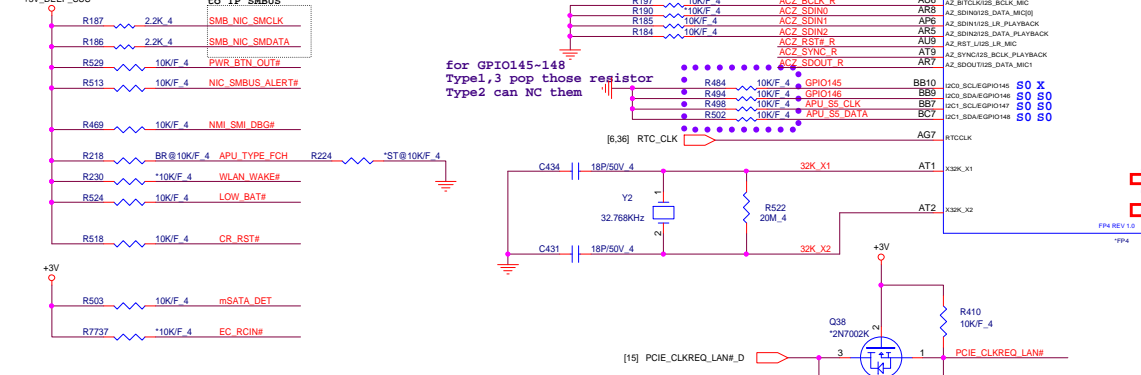
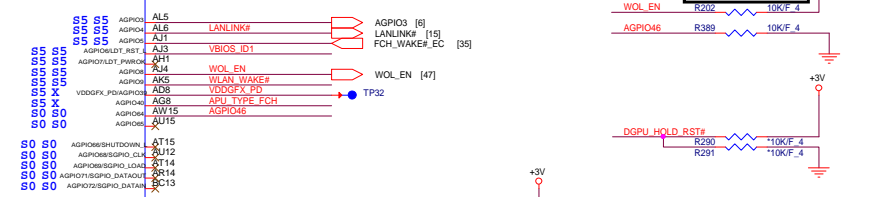
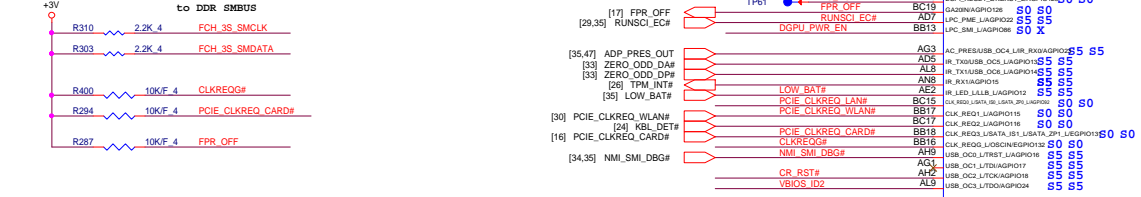
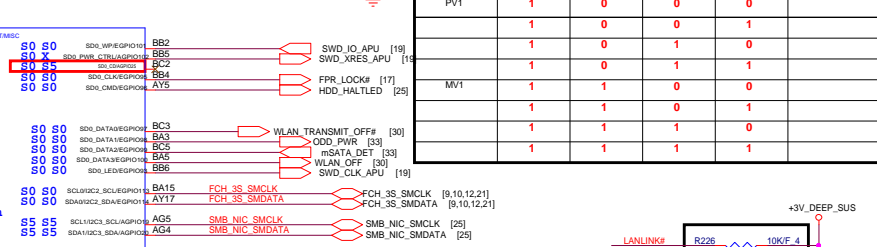
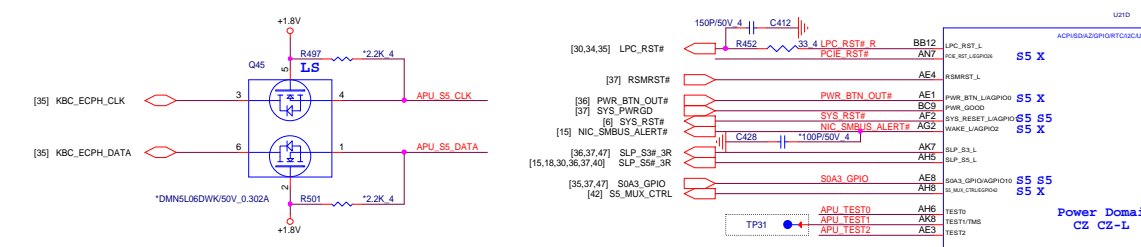
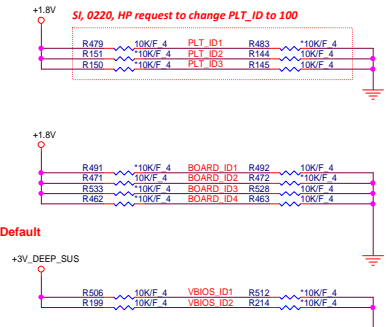




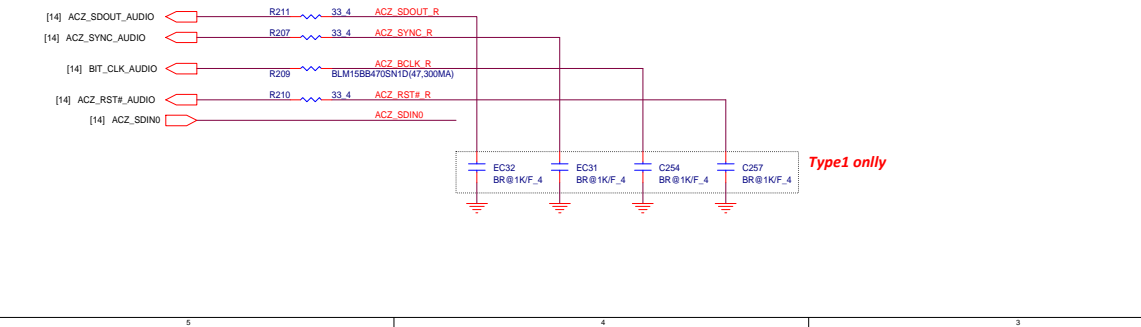
	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	
BOARD REVISION	EGPIO135	EGPIO136	EGPIO137	EGPIO138	
DB0	0	0	0	0	
DB1	0	0	0	1	
DB2	0	0	1	0	
	0	0	1	1	
SI1	0	1	0	0	Default
SI6	0	1	0	1	
SI2	0	1	1	0	
	0	1	1	1	
PV1	1	0	0	0	
	1	0	0	1	
	1	0	1	0	
	1	0	1	1	
MV1	1	1	0	0	
	1	1	0	1	
	1	1	1	0	
	1	1	1	1	



VBIOS_ID	VBIOS_ID1	VBIOS_ID2
	AGPIO6	AGPIO24
Discrete VRAM Group #1	0	0
Discrete VRAM Group #2	0	1
Discrete VRAM Group #3	1	0
UMA	1	1

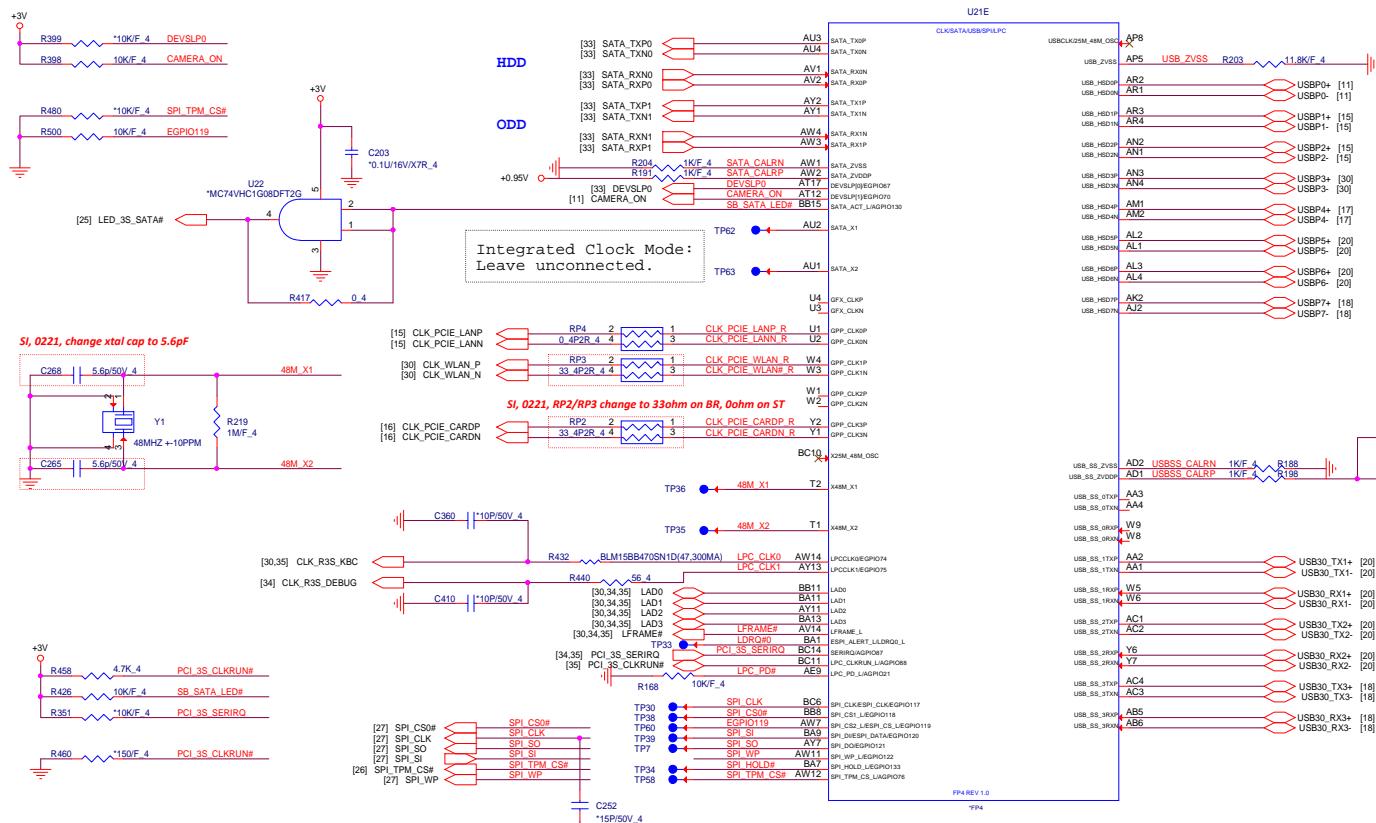


## To Azalia



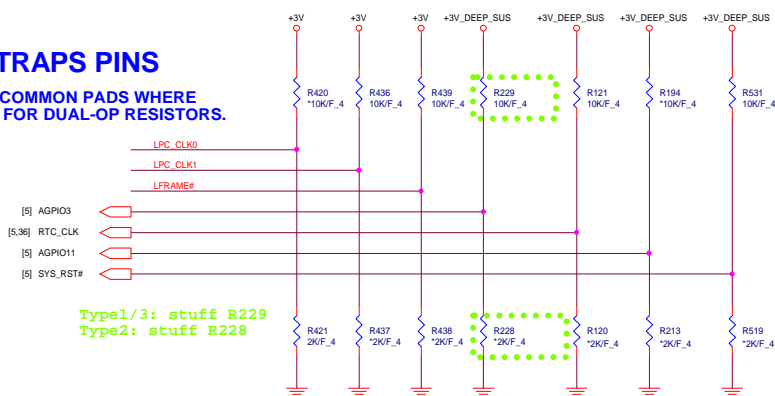
Follow AMD checklist 53537\_1\_03 suggestion to stuff R118/R120/R122

TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



## STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



### REQUIRED STRAPS

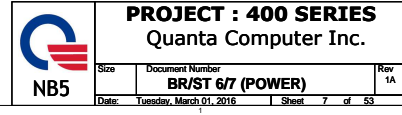
Follow FAE comment: R659 change to 2K, R401 to 10k, R142 is NC

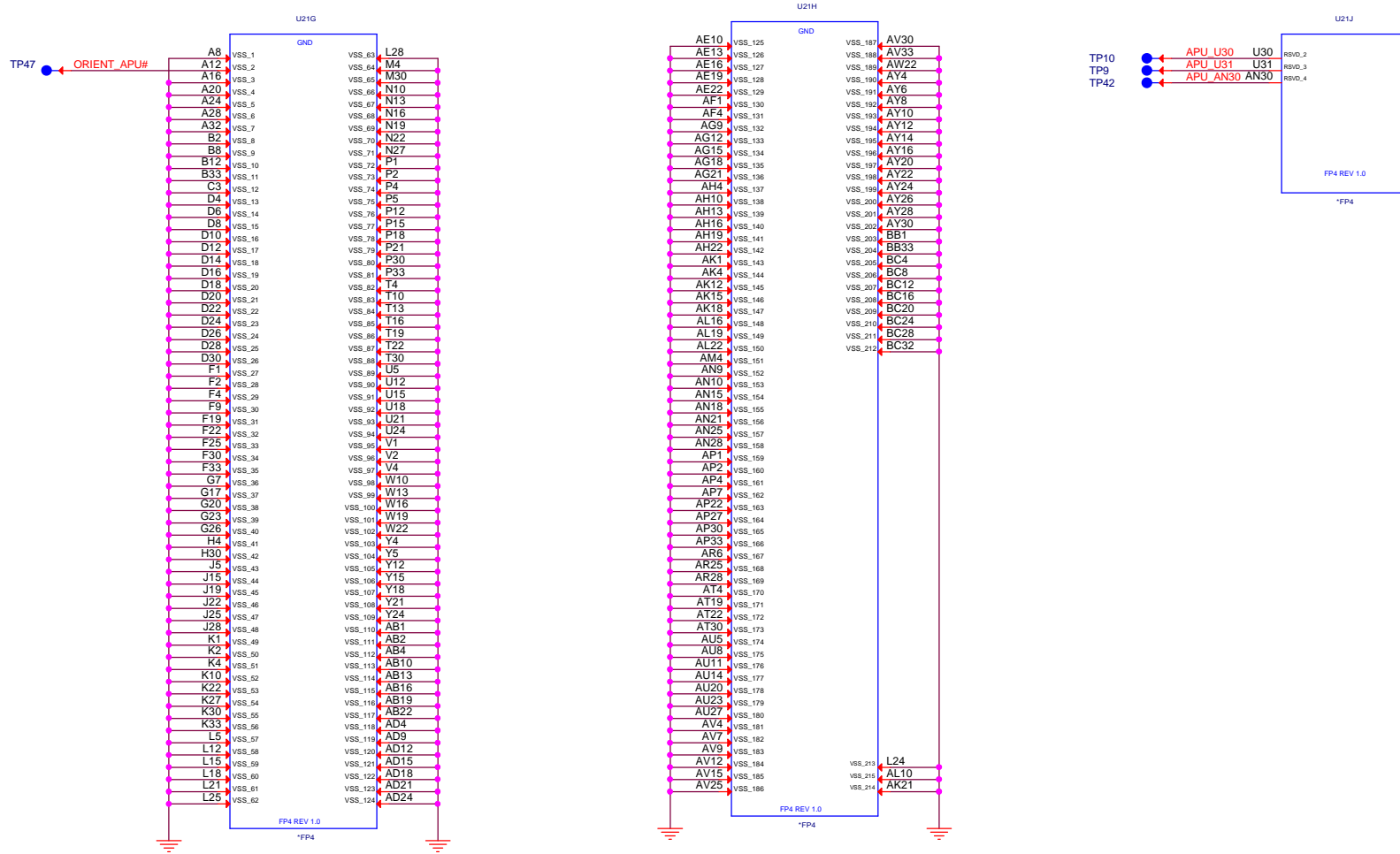
REQUIRED CHIPS		OPTIONAL CHIPS		OPTIONAL CHIPS		OPTIONAL CHIPS		OPTIONAL CHIPS	
	LPC_CLK0	LPC_CLK1	LFRAM#	AGP03 Int Pull-Up	AGP03 Int Pull-Up	RTG_CLK Int Pull-Up	BLINK Int Pull-Up	AGP011 Int Pull-Up	SYS_RST# Int Pull-Up
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48MHz crystal clock and generate both internal and external clocks DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM DEFAULT	Enhanced reset logic (for quicker SS resume) DEFAULT	Coin battery is on board. DEFAULT	LDT_RSTWDT_PWRG0 output to APU DEFAULT	normal reset mode DEFAULT	
PULL LOW	BOOT FAIL TIMER DISABLED	Use 100mHz PCIe clock as reference clock and generate internal clocks only ASLWU	LPC ROM	3.3V SPI ROM DEFAULT	Default to traditional reset logic DEFAULT	Coin battery is not on board. DEFAULT	LDT_RSTWDT_PWRG0 output to Pads DEFAULT	short reset mode DEFAULT	



**PROJECT : 400 SERIES**  
Quanta Computer Inc.

Size	Document Number <b>BR/ST 5/7 (SATA/USB/SPI)</b>	Rev 1A
Date: Tuesday, March 01, 2016		Sheet 6 of 53

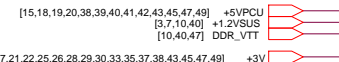
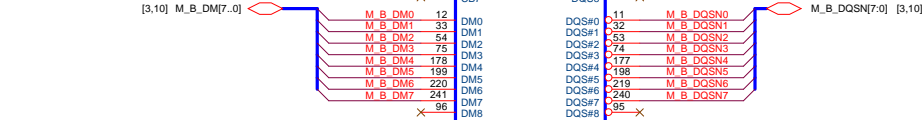




**PROJECT : 400 SERIES**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>BR/ST 7/7 (GND)</b>	<b>1A</b>
Date: Tuesday, March 01, 2016		Sheet 8 of 53



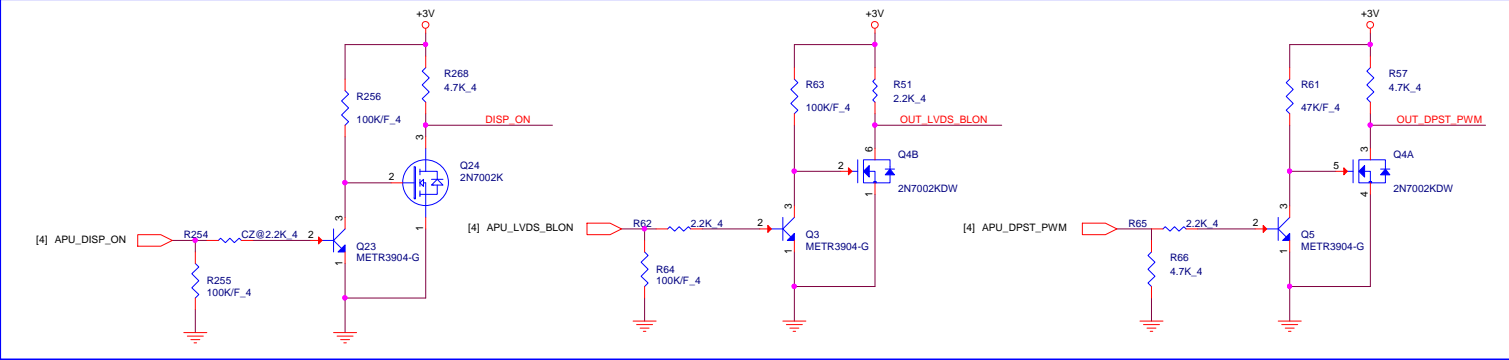
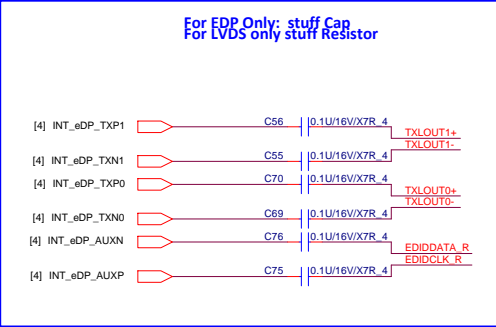
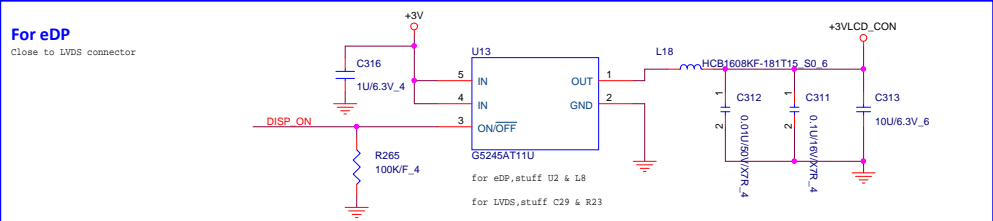
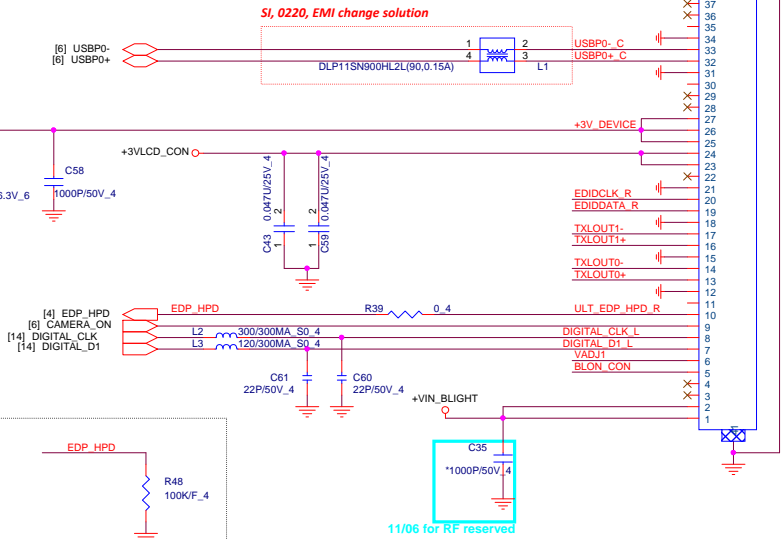
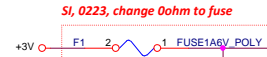
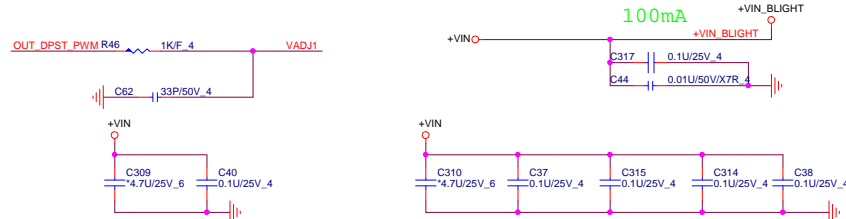
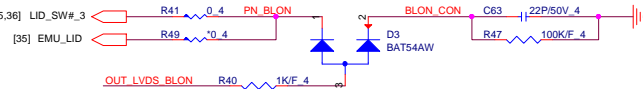
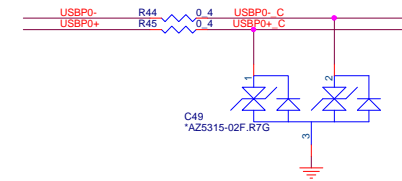
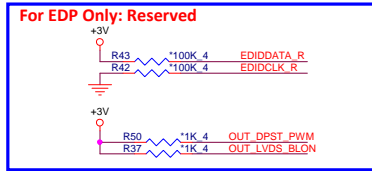




# LID Switch

11

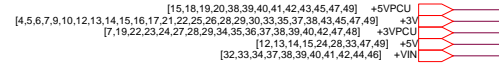
LVDS Conn.

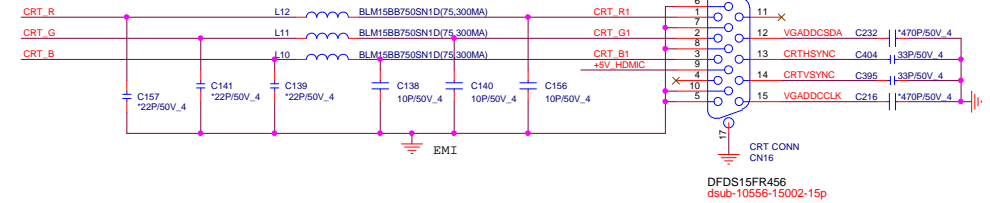
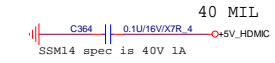
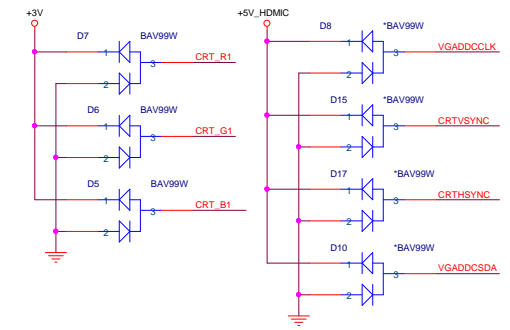
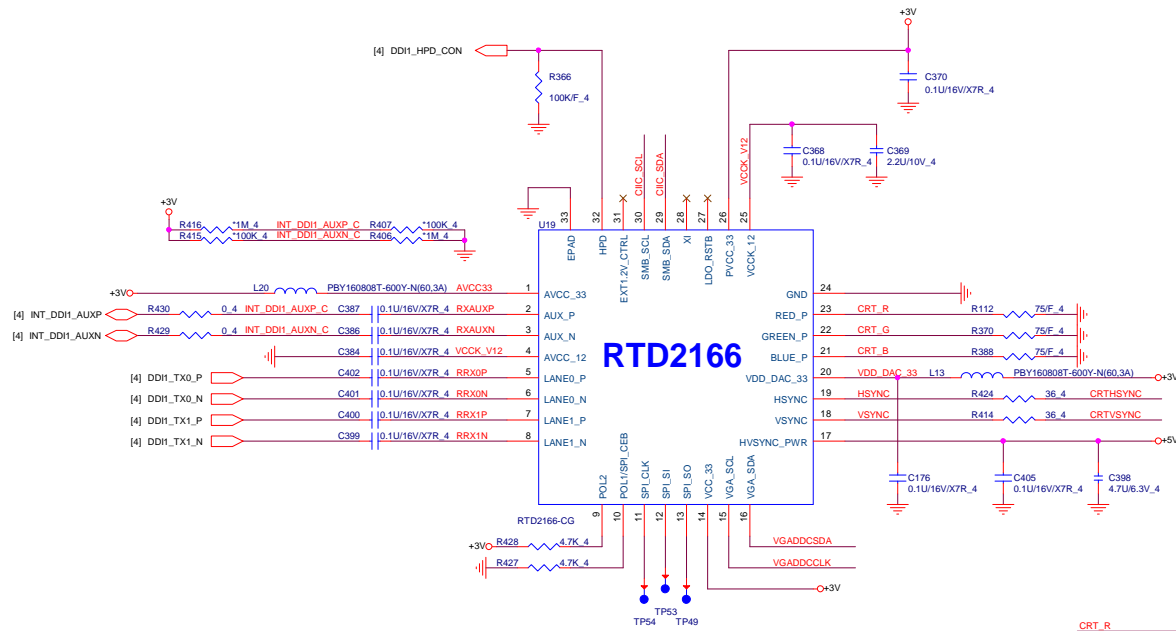


**PROJECT : 400 SERIES**  
Quanta Computer Inc.

Size Custom Document Number LCD CONN/LID/CAM/D-MIC Rev 1A

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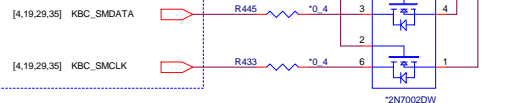
### CIIC\_SCL, CIIC\_SDA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS  
 ROM or EEPROM mode: connect to PCH SMBUS  
 IIC Protocol is used

#### From PCH



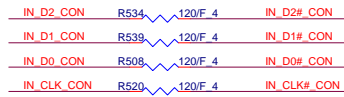
#### From EC



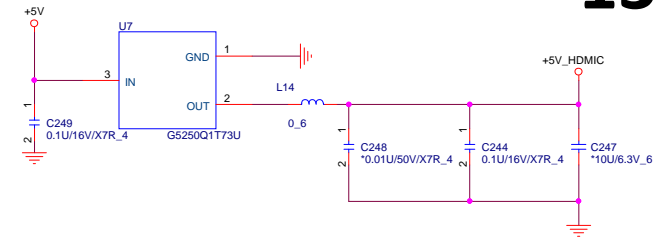
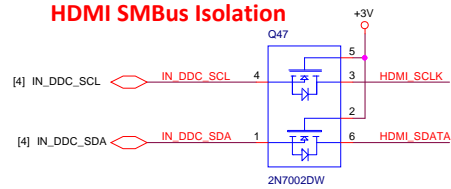
**PROJECT : 400 SERIES**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	DP to VGA	1A
Date: Tuesday, March 01, 2016	Sheet 12 of 53	

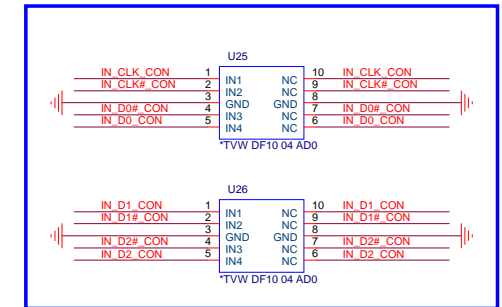
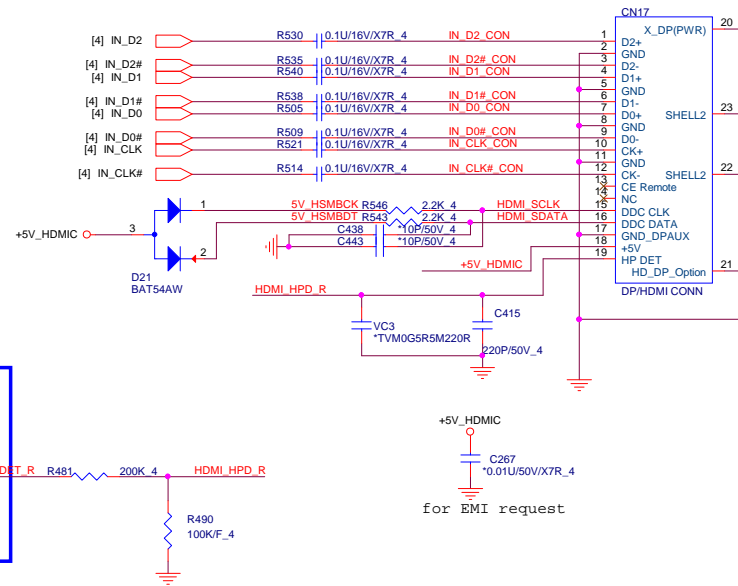
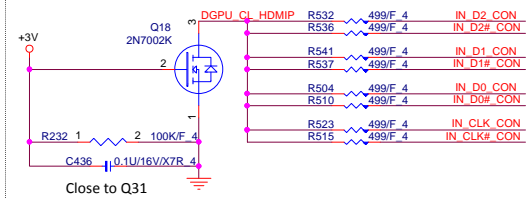
## EMI Solution



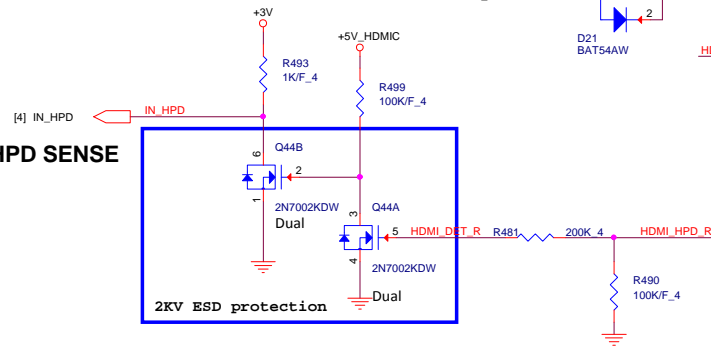
## HDMI SMBus Isolation

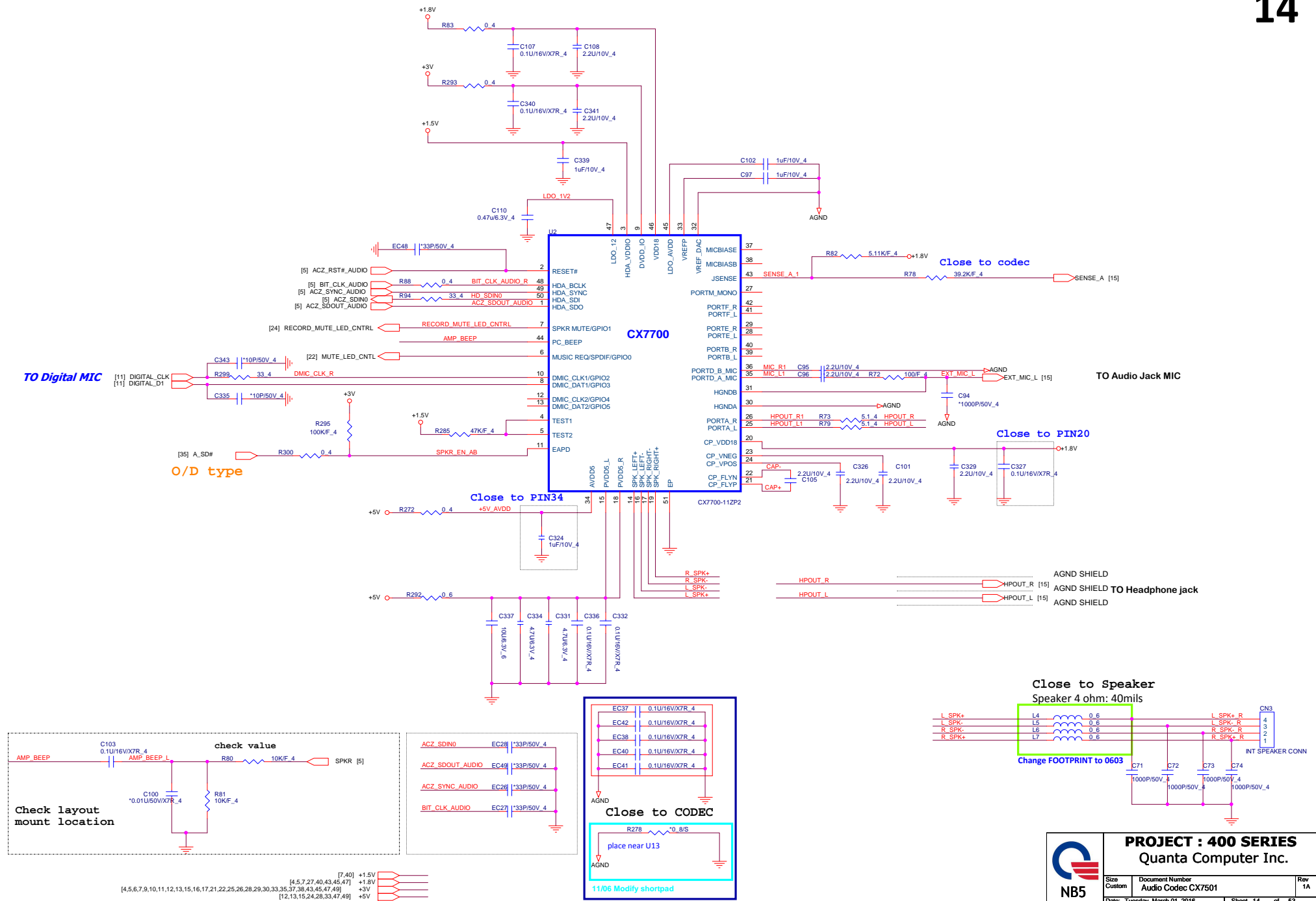


**Close to HDMI connector**

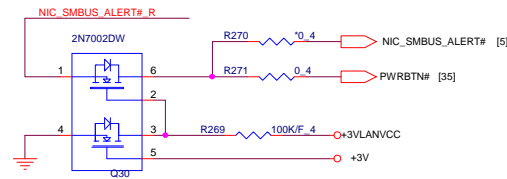
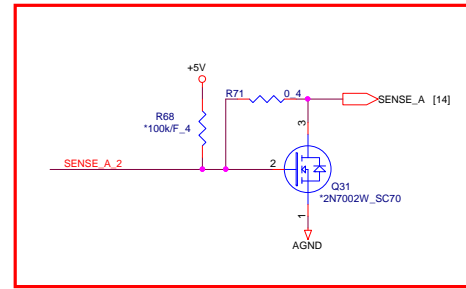
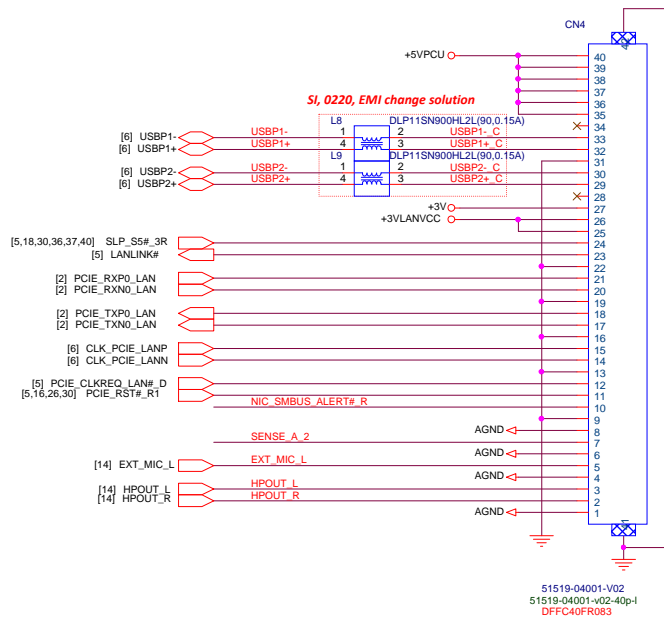


## HDMI HPD SENSE



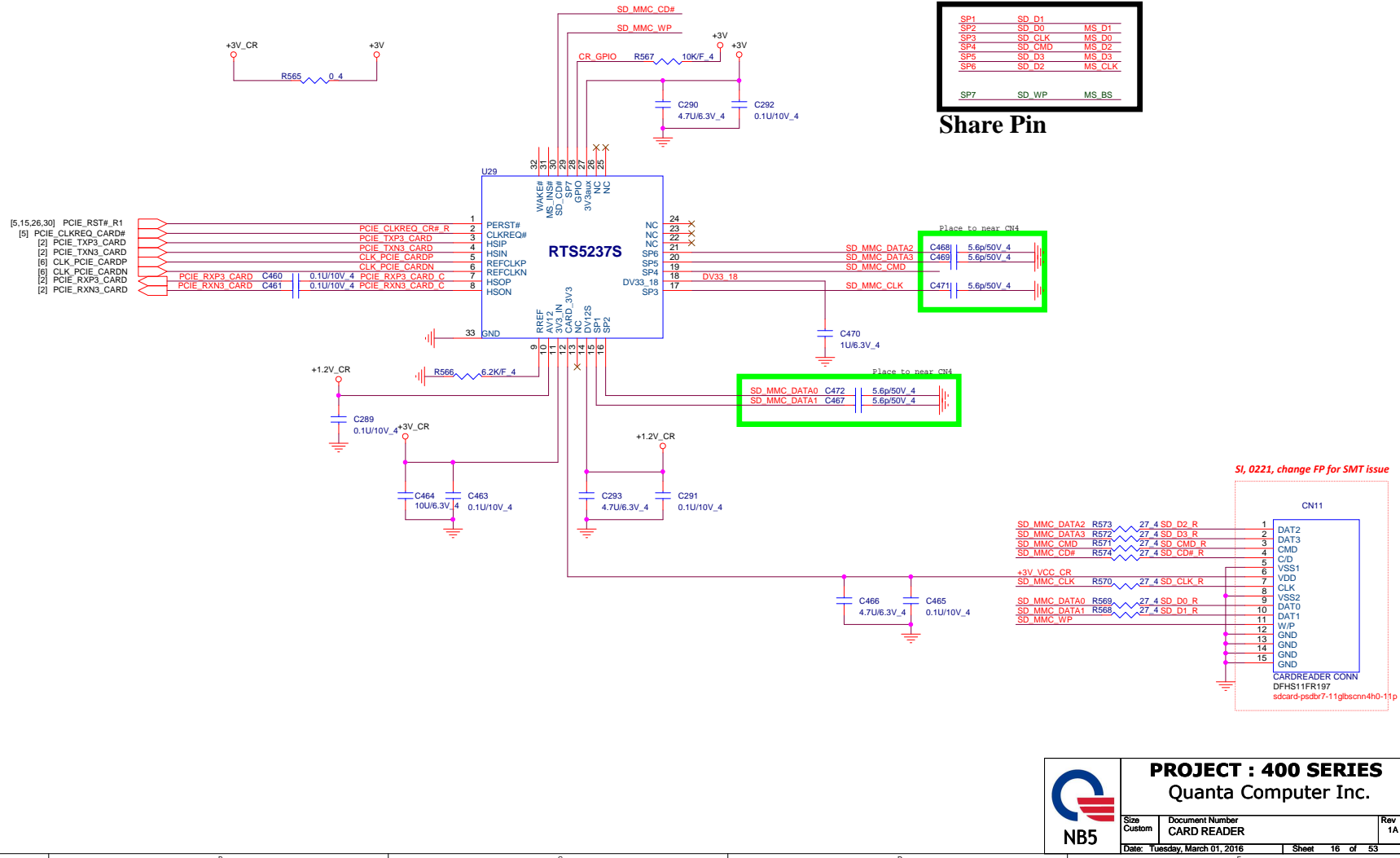


# USB2.0 x2/LAN/Headphone\_Mic Combo Jack Daughter Board Connector

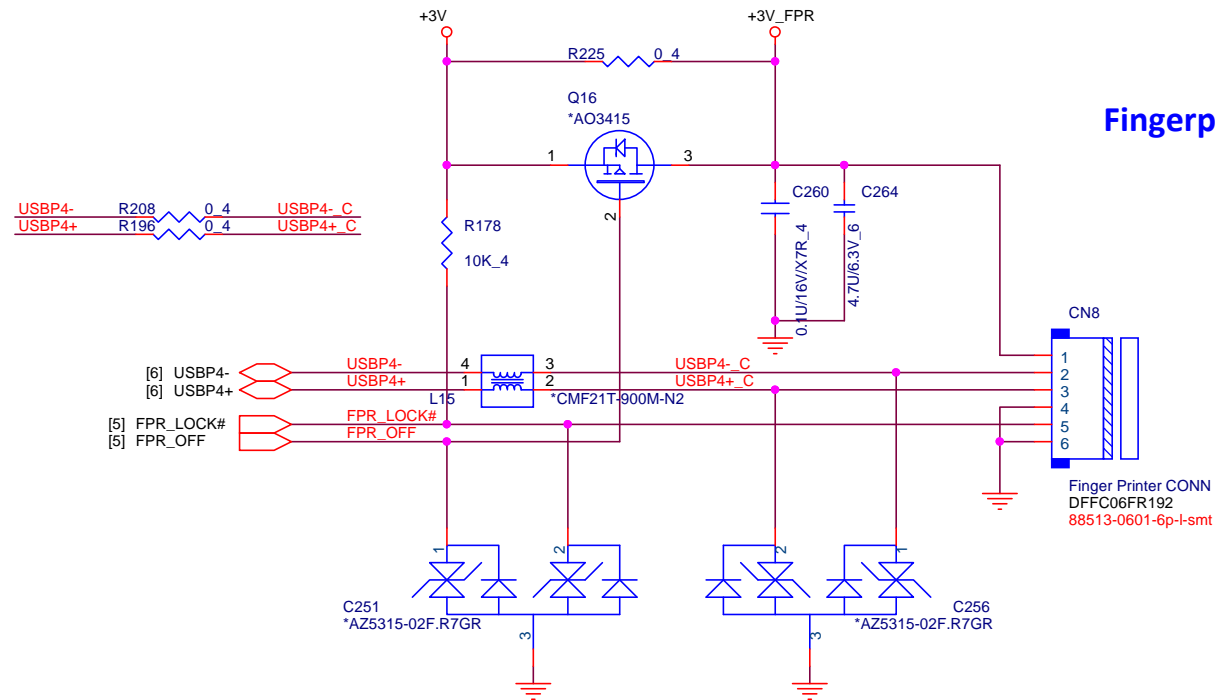


**PROJECT : 400 SERIES**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Audio/USB BOARD	1A
Date: Tuesday, March 01, 2016	Sheet 15 of 53	







**PROJECT : 400 SERIES**  
Quanta Computer Inc.

Size Custom	Document Number <b>Finger Printer</b>	Rev 1A
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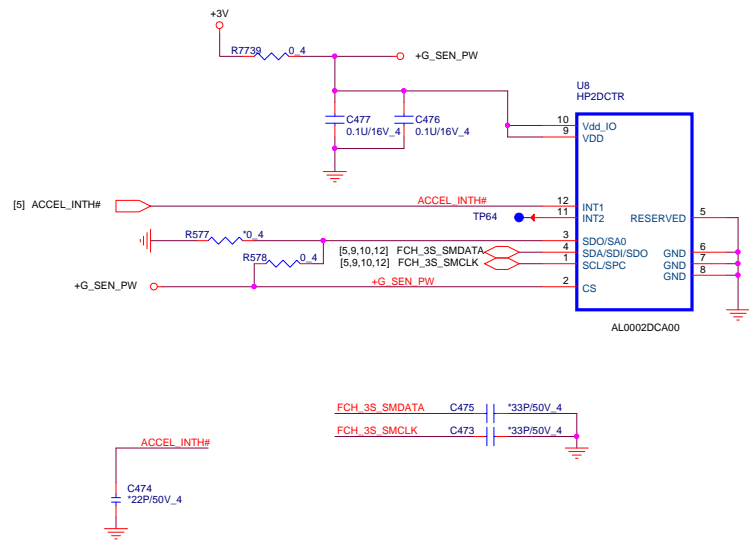
Date: Tuesday, March 01, 2016 Sheet 17 of 53








Accelerometer Sensor

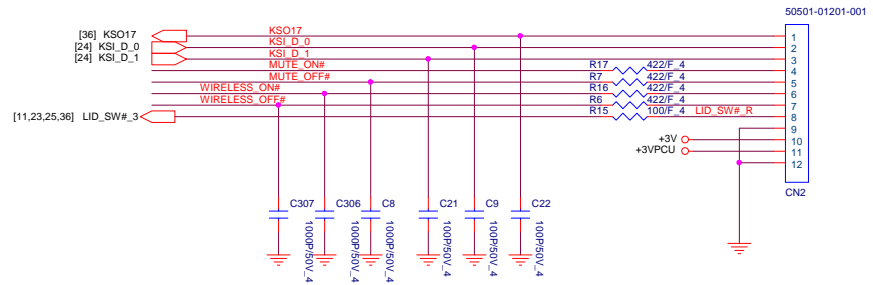


[15,18,19,20,38,39,40,41,42,43,45,47,49] +5VPCU  
[7,19,22,23,24,27,28,29,34,35,36,37,38,39,40,42,47,48] +3VPCU

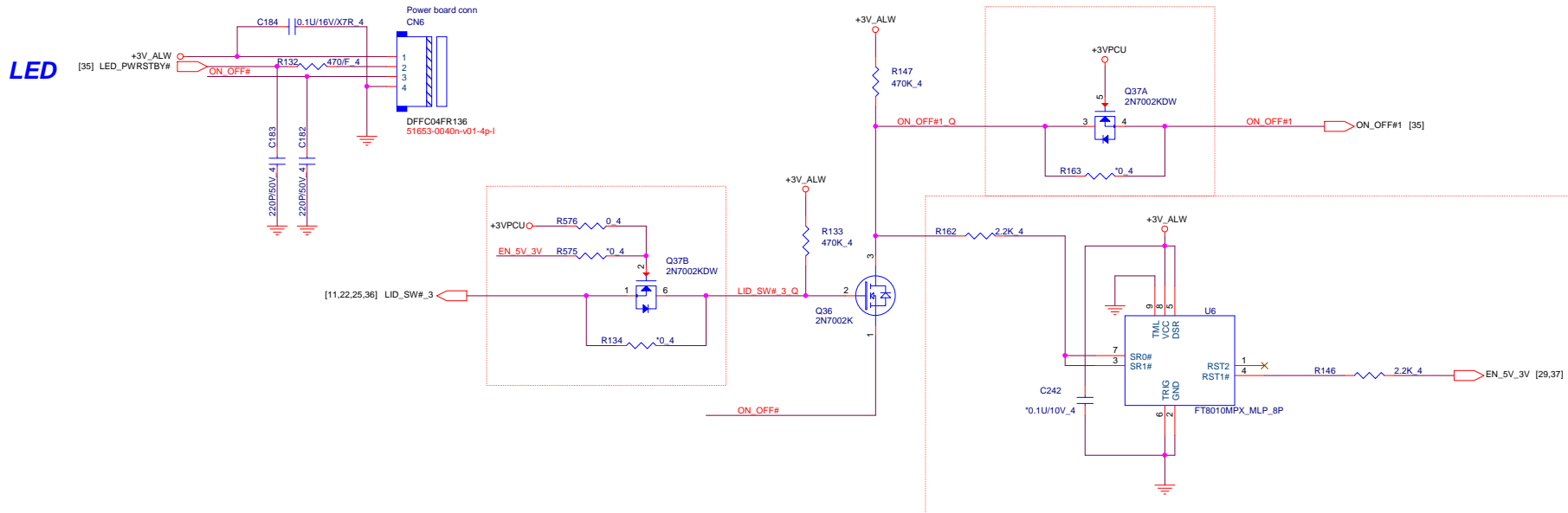


**PROJECT : 400 SERIES**  
Quanta Computer Inc.


Size Custom	Document Number <b>Accelerometer</b>	Rev 1A
Date: Tuesday, March 01, 2016	Sheet 21 of 53	



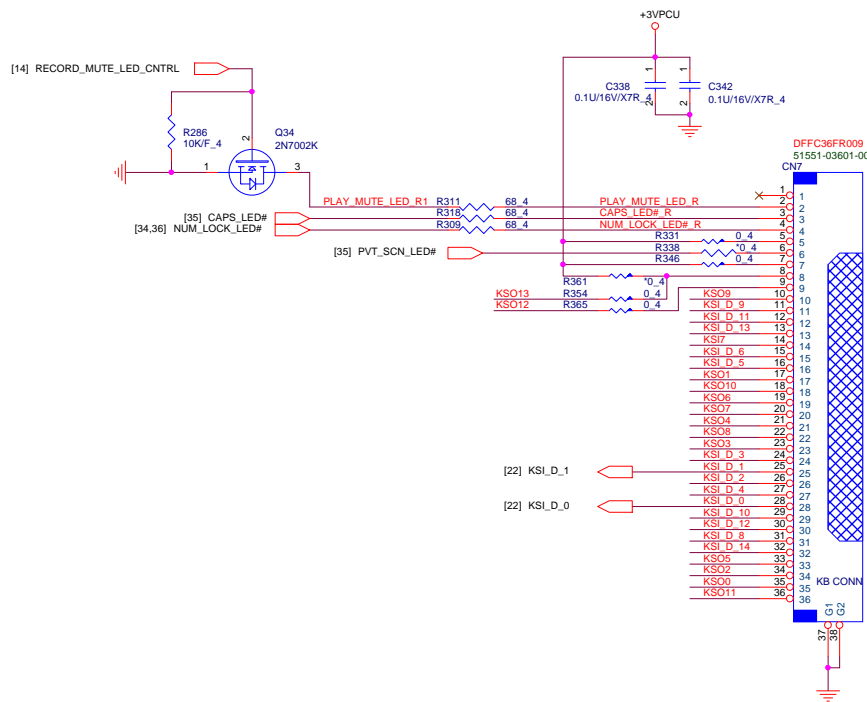
## Power Botton Connector



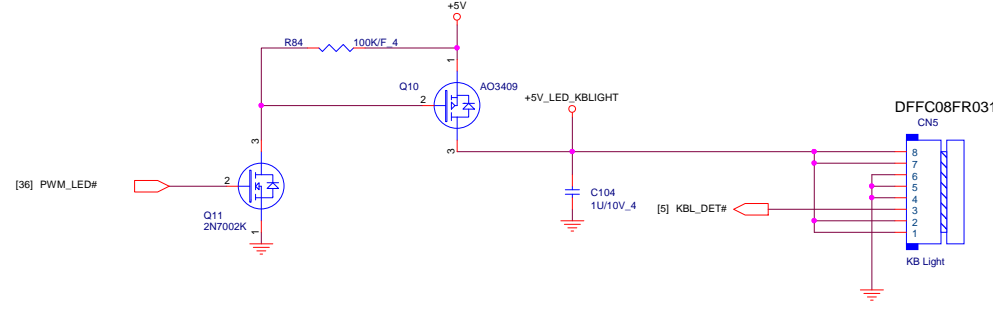
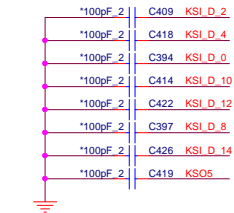
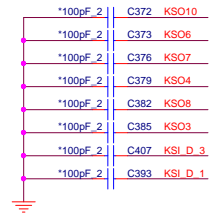
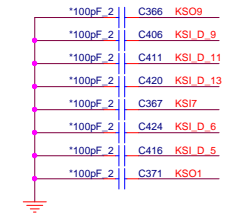
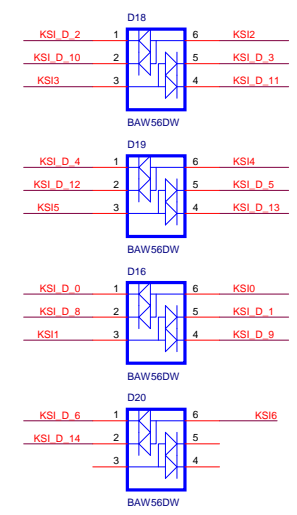
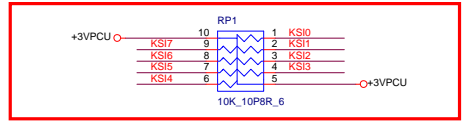
[37,38,39,48] +3V\_ALW  
 [4,5,6,7,9,10,11,12,13,14,15,16,17,21,22,25,26,28,29,30,33,35,37,38,43,45,47,49] +3V  
 [12,13,14,15,24,28,33,47,49] +5V  
 [7,19,22,24,27,28,29,34,35,36,37,38,39,40,42,47,48] +3VPCU

		<b>PROJECT : 400 SERIES</b>	
		<b>Quanta Computer Inc.</b>	
Size Custom	Document Number <b>33 -- PB/LID</b>	Rev 1A	
Date: Tuesday, March 01, 2016	Sheet 23 of 53		

# KEYBOARD Con.



## KEYBOARD PULL-UP

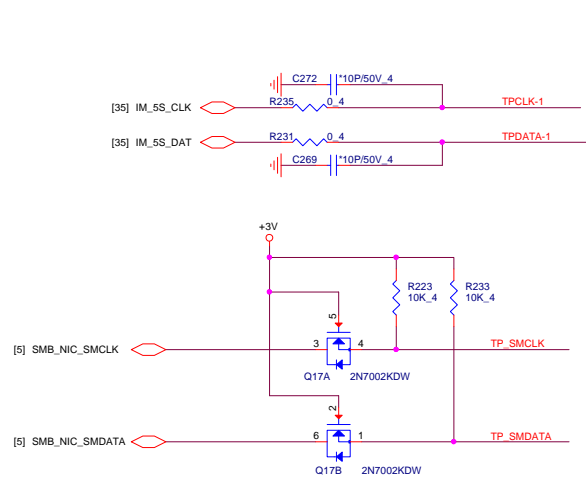


[4,5,6,7,9,10,11,12,13,14,15,16,17,21,22,25,26,28,29,30,33,35,37,38,43,45,47,48] +3V  
 [12,13,14,15,28,33,47,49] +5V  
 [7,19,22,23,27,28,29,34,35,36,37,38,39,40,42,47,48] +3VPCU

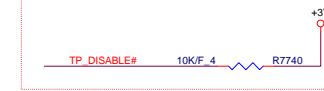
**PROJECT : 400 SERIES**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>KB/KB light</b>	Rev 1A
Date: Tuesday, March 01, 2016	Sheet 24 of 53	

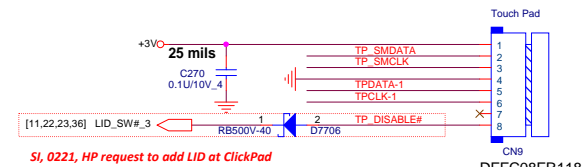




SI, 0221, HP request to add LID at ClickPad

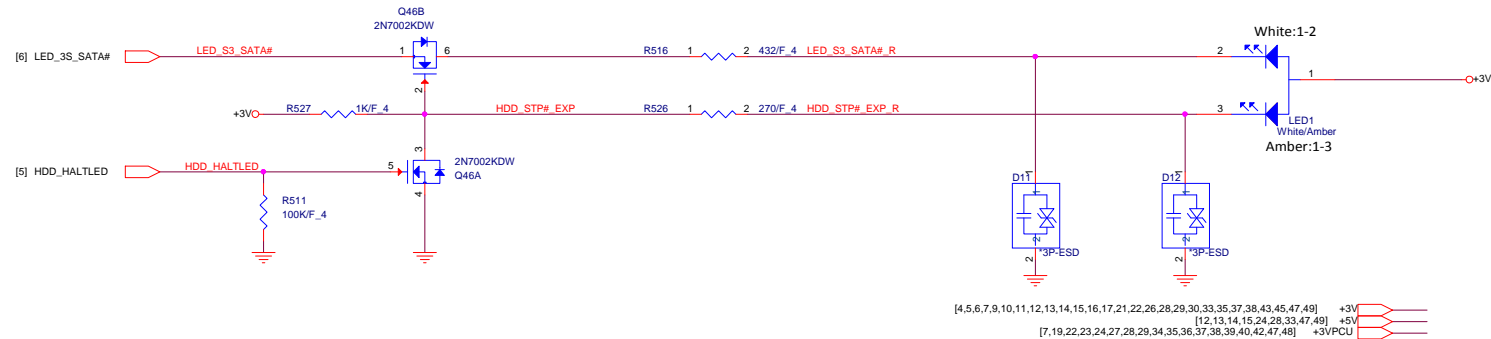


### Touch POINT



SI, 0221, HP request to add LID at ClickPad

**CLICK PAD**  
Address: 0x2C(7 bit)

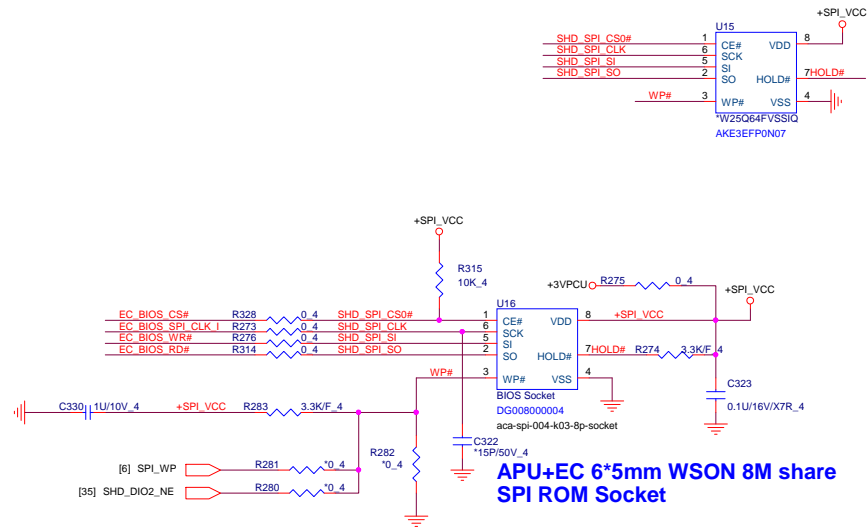


**PROJECT : 400 SERIES**  
**Quanta Computer Inc.**

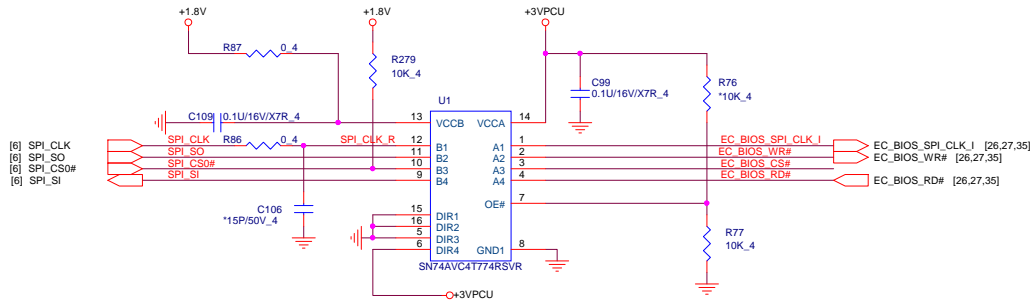
Size	Document Number	Rev
Custom	34 -- Forced Pad/Card reader	1A
Date: Tuesday, March 01, 2016	Sheet 25 of 53	




Size Custom	Document Number <b>TPM SLB9665_QFN</b>	Rev 1A
Date: Tuesday, March 01, 2016		Sheet 26 of 53

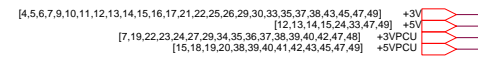
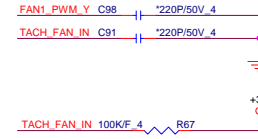
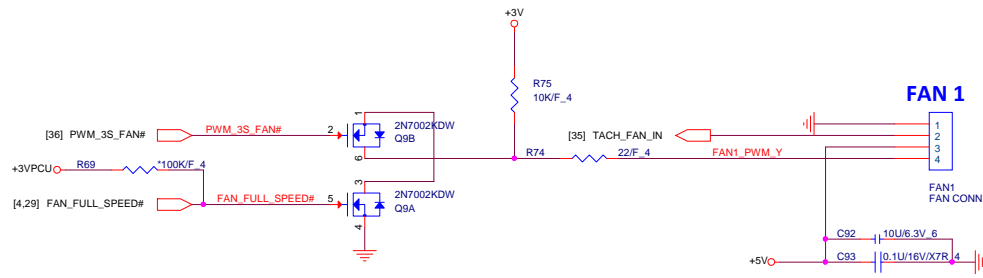



From EC

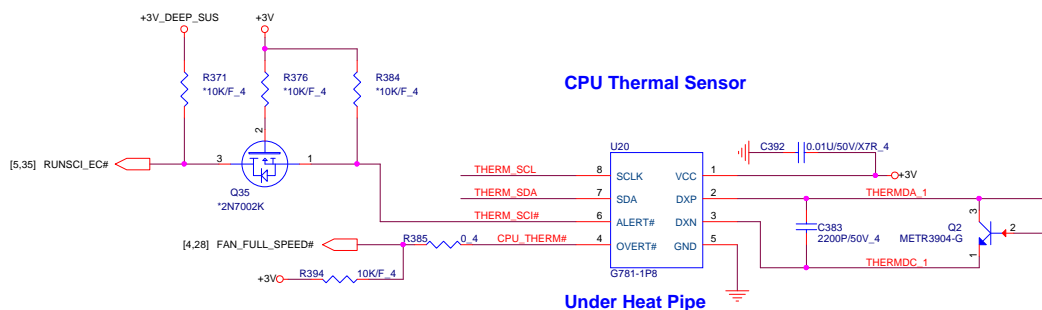


OE#	DIR	OPERATION
L	L	B TO A
L	H	A TO B
H	X	Disconnect

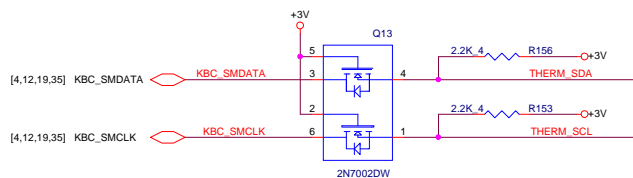
		<b>PROJECT : 400 SERIES</b> Quanta Computer Inc.	
Size Custom	Document Number Flash(KBC+PCH)	Rev 1A	
Date: Tuesday, March 01, 2016	Sheet 27 of 53		



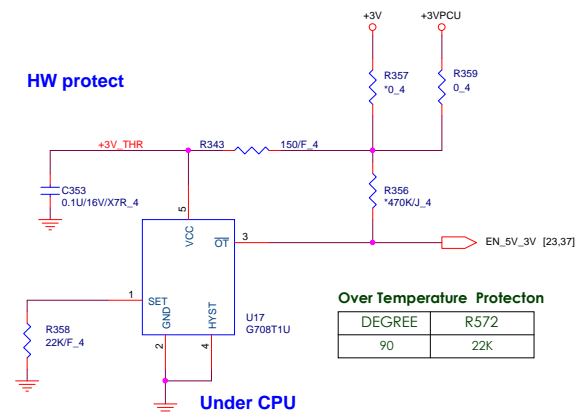
		<b>PROJECT : 400 SERIES</b> <b>Quanta Computer Inc.</b>	
		Size Custom Document Number <b>35 -- FAN</b>	Rev 1A
Date: Tuesday, March 01, 2016		Sheet 28 of 53	E



1st: AL000781039 G781-1P8(9Ah)  
2nd: AL000431019 TMP431BDGKR(9Ah)



HW protect



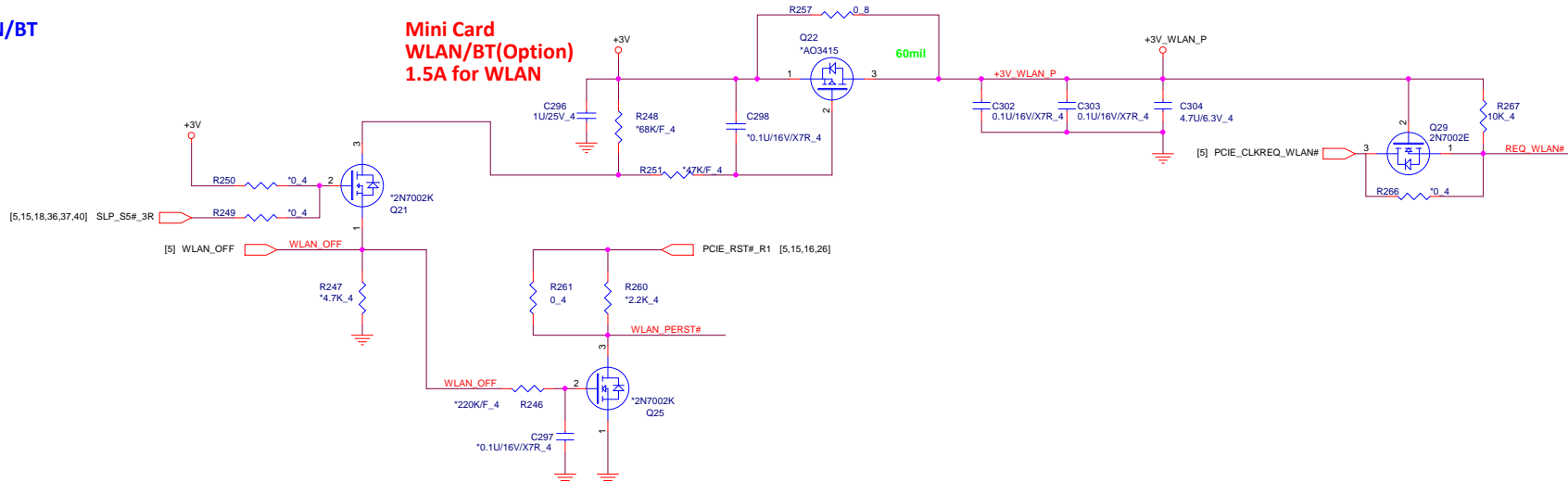
Over Temperature Protection

DEGREE	R572
90	22K

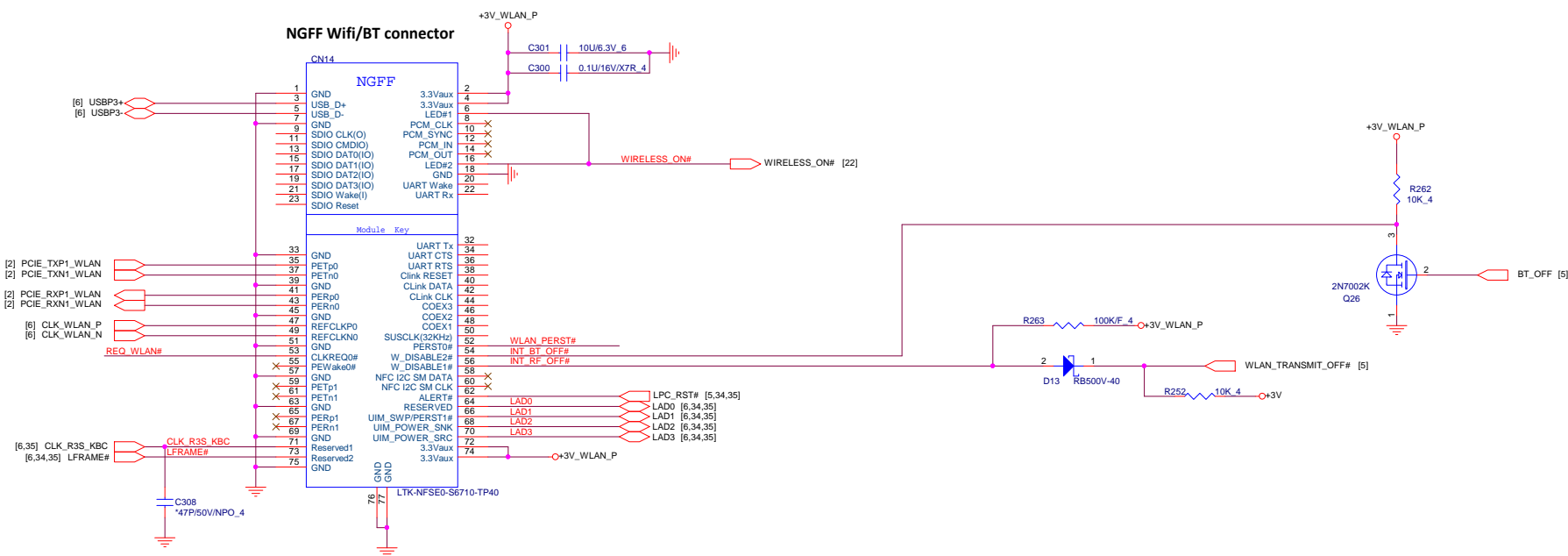
$$RSET (K OHM) = 0.0012T^2 - 0.9308T + 96.147$$

[4,5,6,7,9,10,11,12,13,14,15,16,17,21,22,25,26,28,30,33,35,37,38,43,45,47,49] +3V  
[7,19,22,23,24,27,28,34,35,36,37,38,39,40,42,47,48] +3VPCU

# Mini Card WLAN/BT(Optional) 1.5A for WLAN



## NGFF Wifi/BT connector

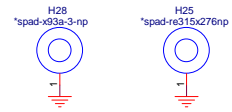


[4,5,6,7,9,10,11,12,13,14,15,16,17,21,22,25,26,28,29,33,35,37,38,43,45,47,49] +3V  
 [12,13,14,15,24,28,33,47,49] +5V  
 [7,19,22,23,24,27,28,29,34,35,36,37,38,39,40,42,47,48] +3VPCU

DB0, 1105, HP confirm to use HDD to M.2 SSD, so delete M.2 SSD related circuit



## EMI PAD

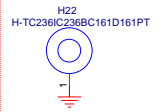


## CPU BKT



SI, 0221, ME change WLAN Nut

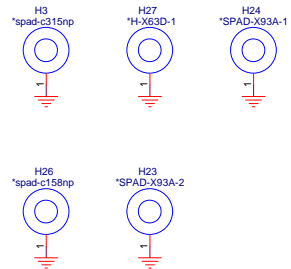
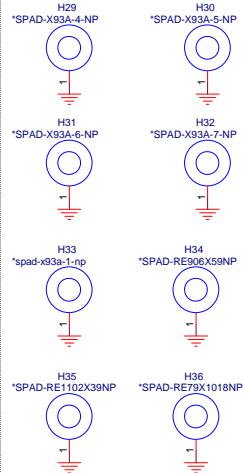
## WLAN NUT



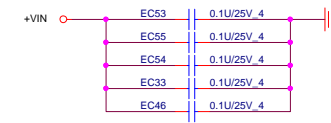
## USBC



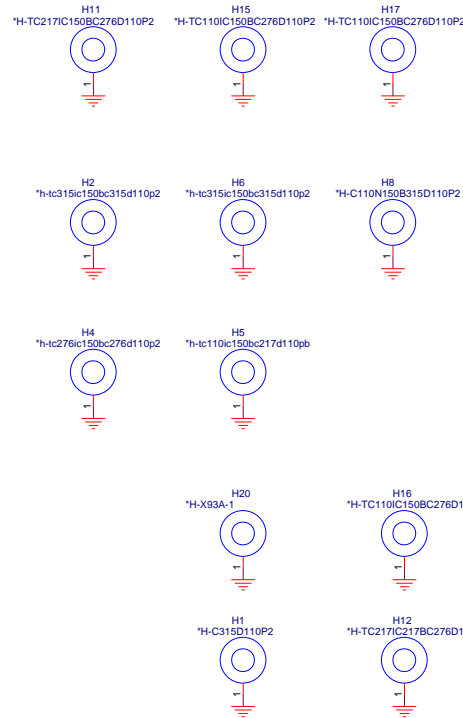
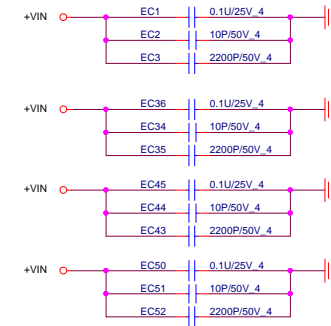
## SPAD



## EMI



## RF

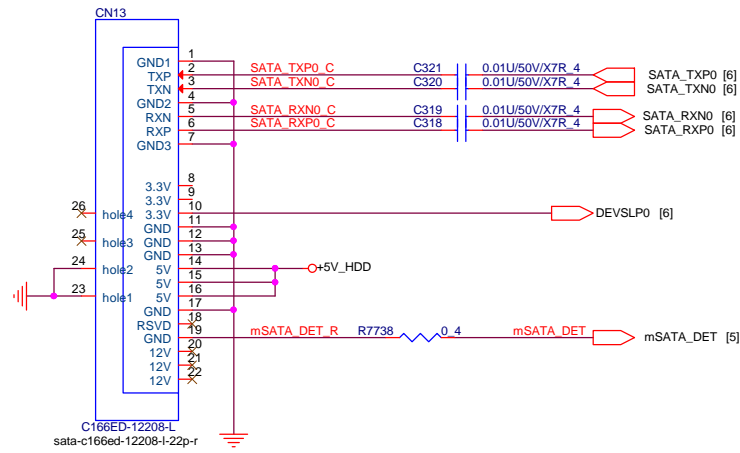


**PROJECT : 400 SERIES**  
**Quanta Computer Inc.**

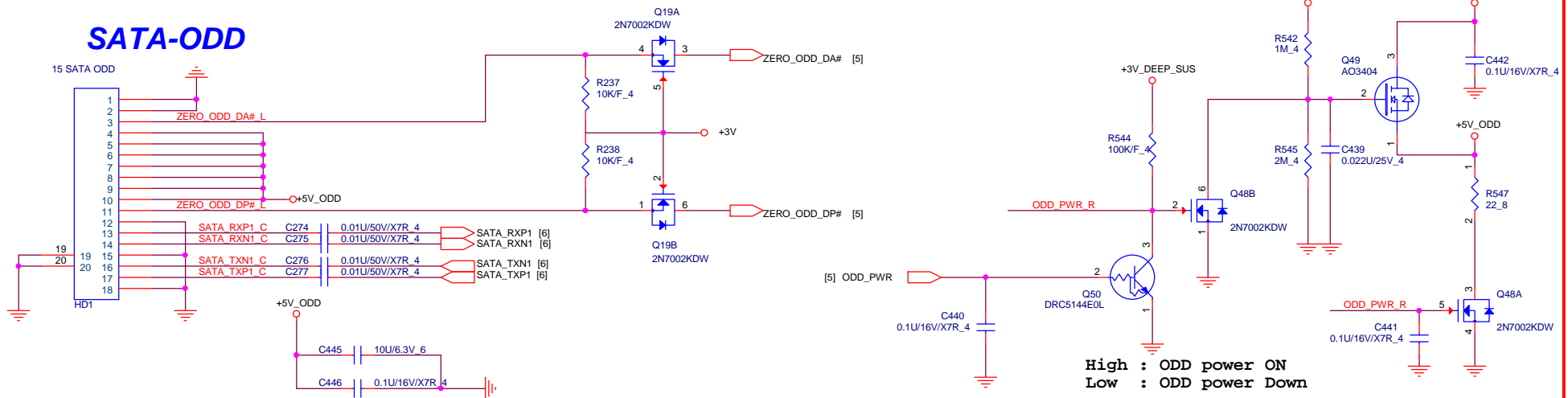
Size	Document Number	Rev
Custom	HOLE	1A
Date: Tuesday, March 01, 2016	Sheet 32 of 53	



## SATA-HDD



## SATA-ODD



[4,5,6,7,9,10,11,12,13,14,15,16,17,21,22,25,26,28,29,30,35,37,38,43,45,47,49] +3V  
[12,13,14,15,24,28,47,49] +5V  
[7,19,22,23,24,27,28,29,34,35,36,37,38,39,40,42,47,48] +3VPCU



**PROJECT : 400 SERIES**  
**Quanta Computer Inc.**

Size B	Document Number <b>37 -- HDD/ODD</b>	Rev 1A
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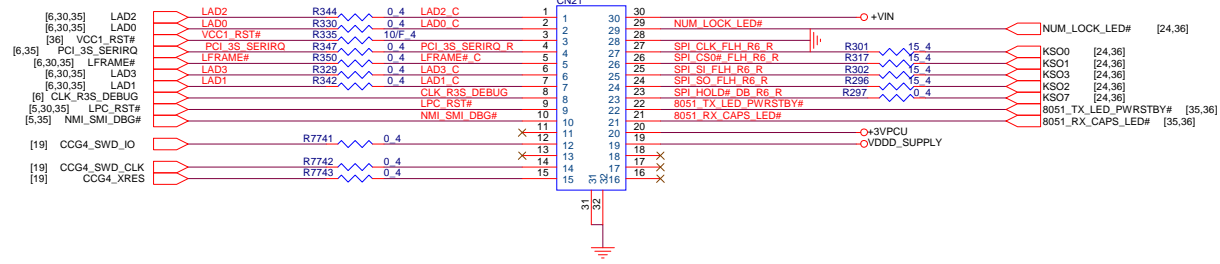
# LPC+EC+CCG4 debug conn on MB

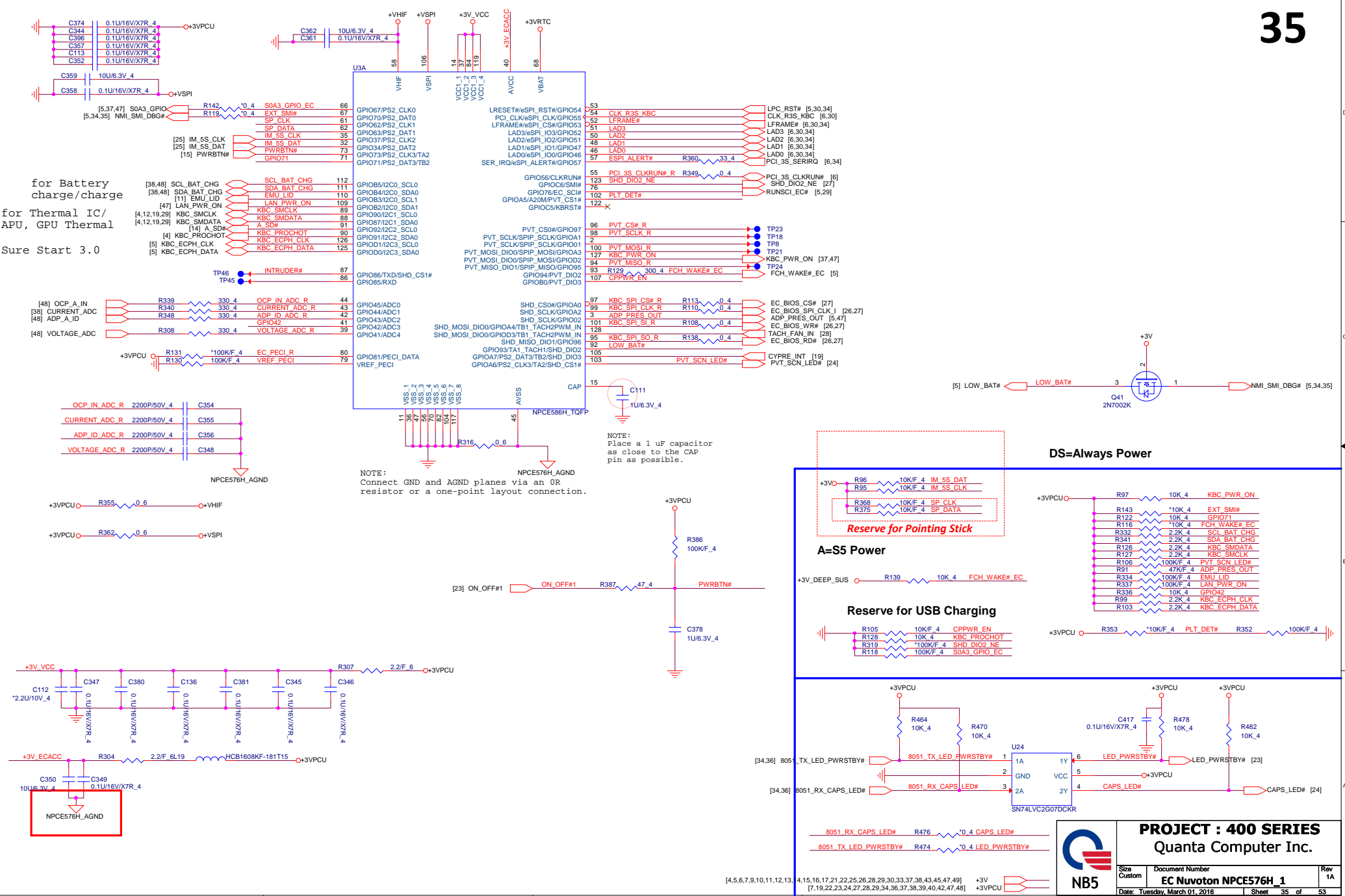
LPC

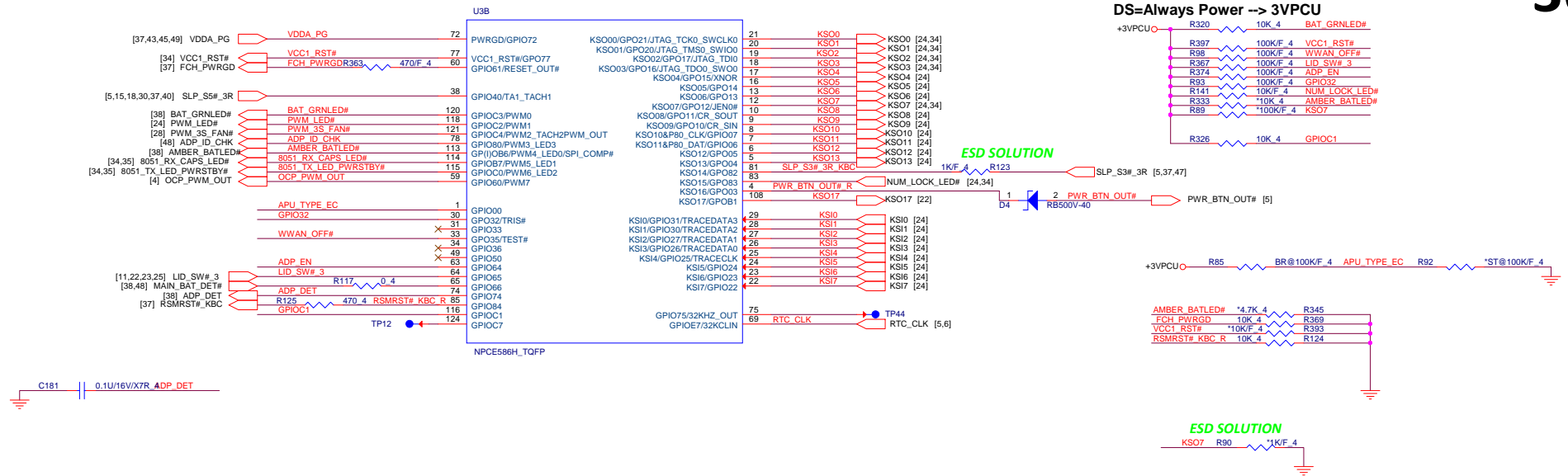
CCG4

EC

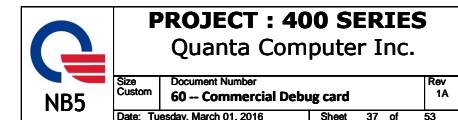
CCF4







# 37

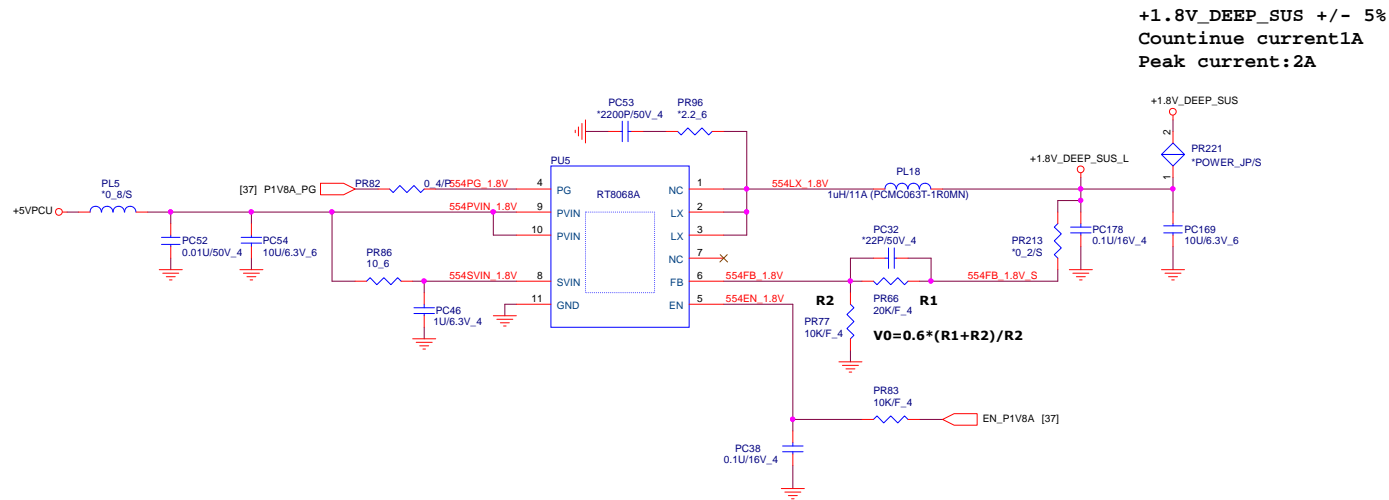
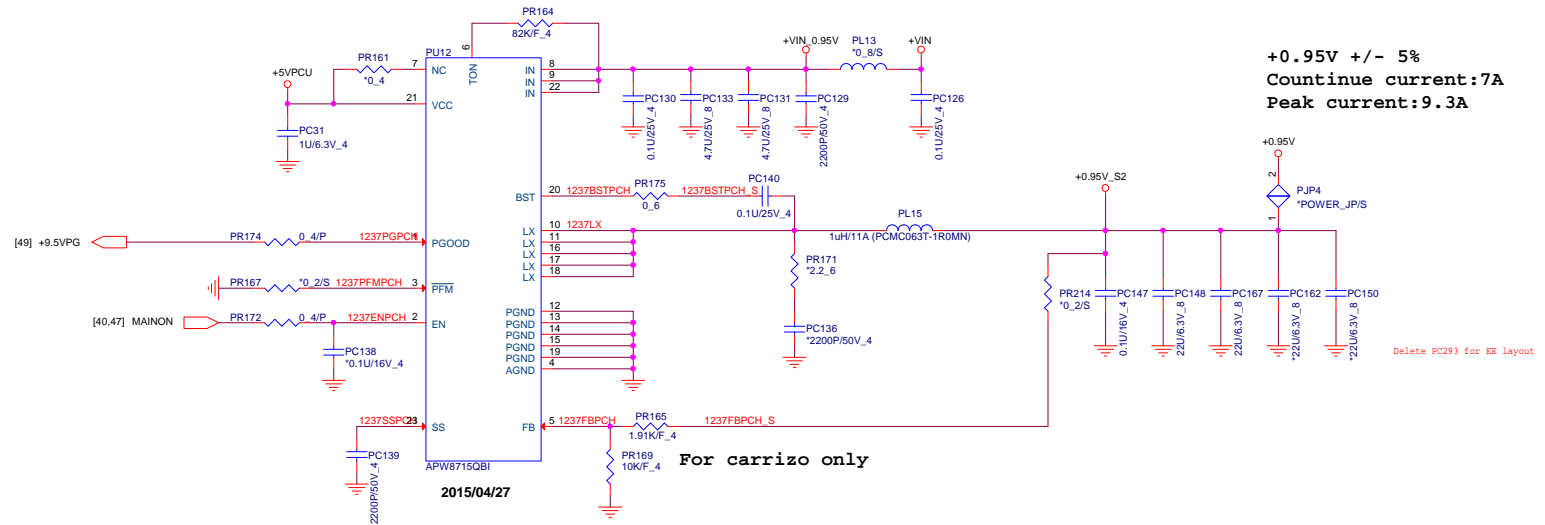





[illegible]



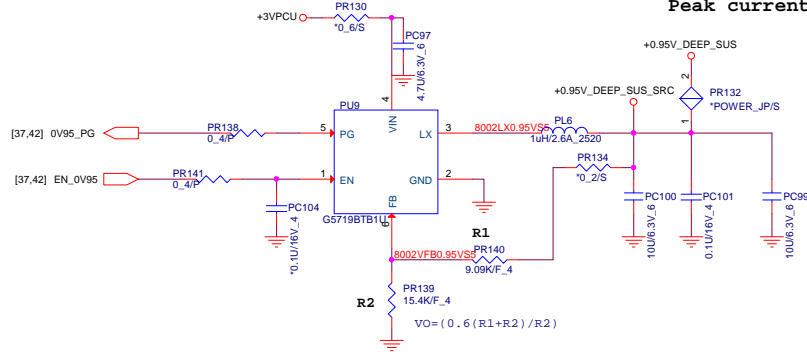




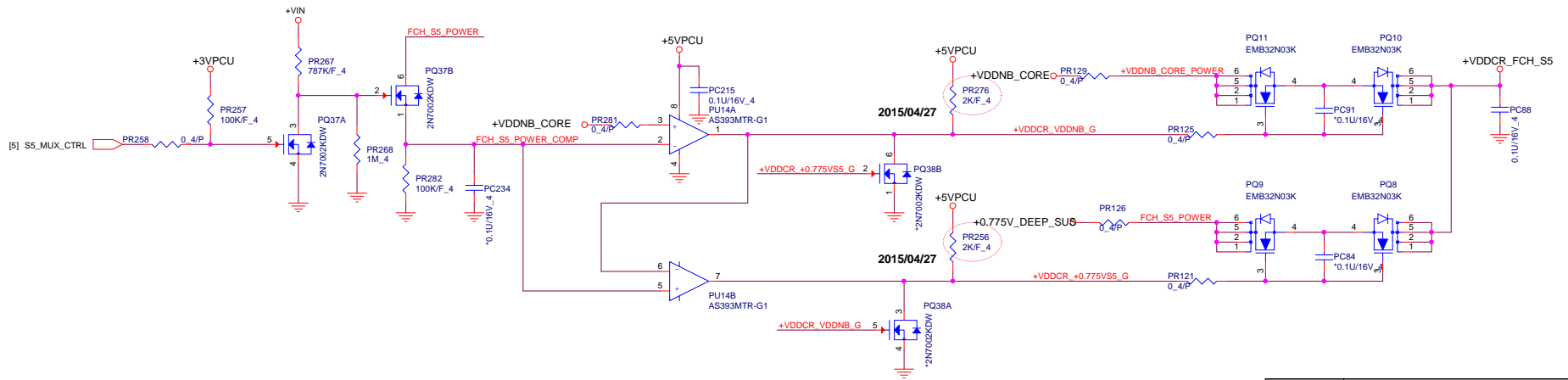
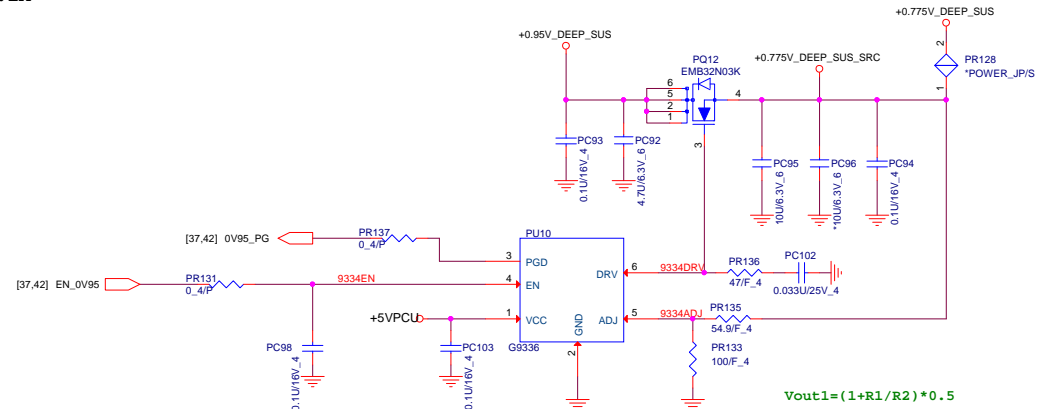
+VIN [11,32,33,34,37,38,39,40,42,44,46]  
+3VPCU [7,19,22,23,24,27,28,29,34,35,36,37,38,39,40,42,44,46]  
+5VPCU [15,18,19,20,38,39,40,42,43,45,47,49]

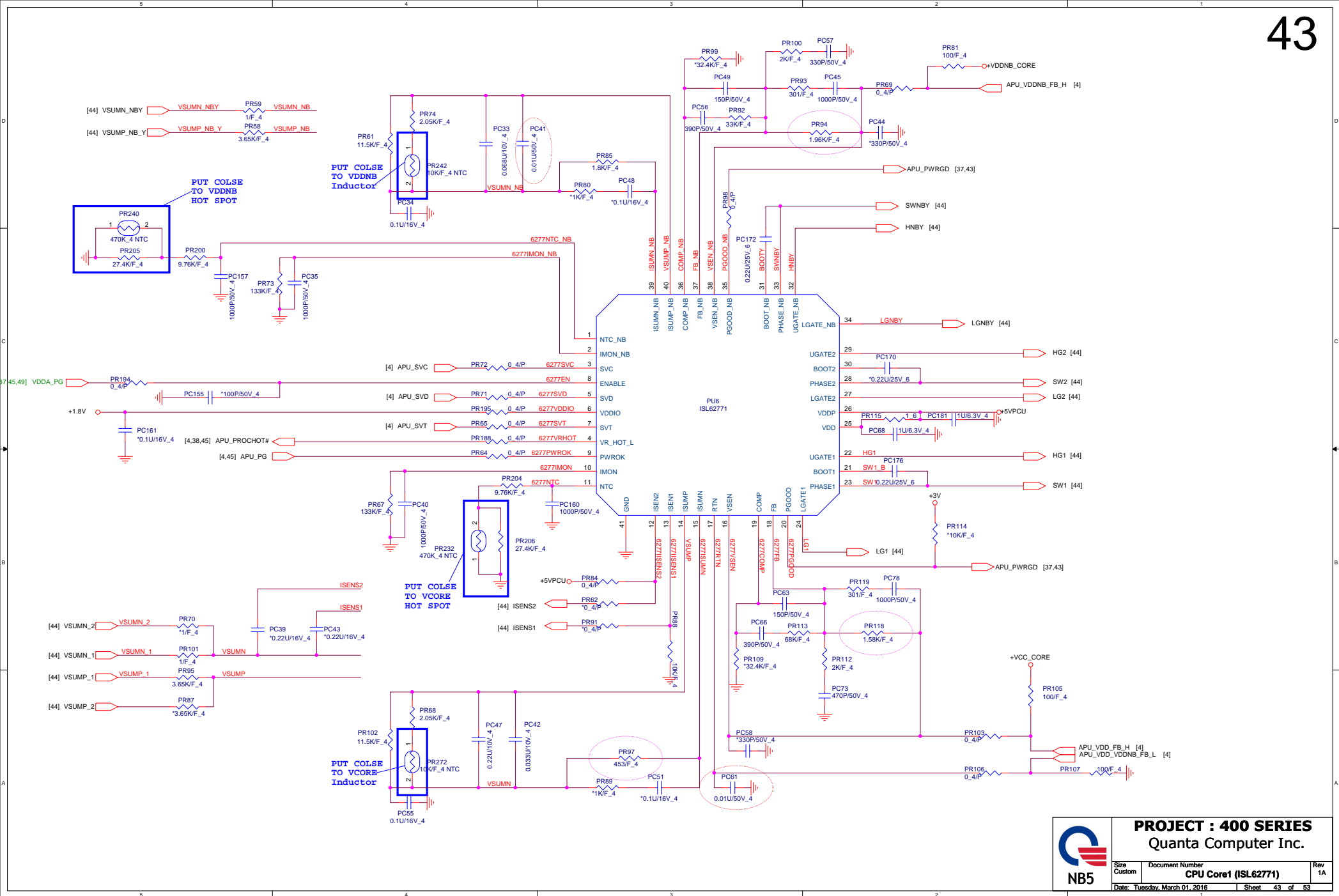
		<b>PROJECT : 400 SERIES</b>	
		<b>Quanta Computer Inc.</b>	
Size Custom	Document Number <b>+1.1VS5 (RT8228)/2.5V</b>	Rev 1A	
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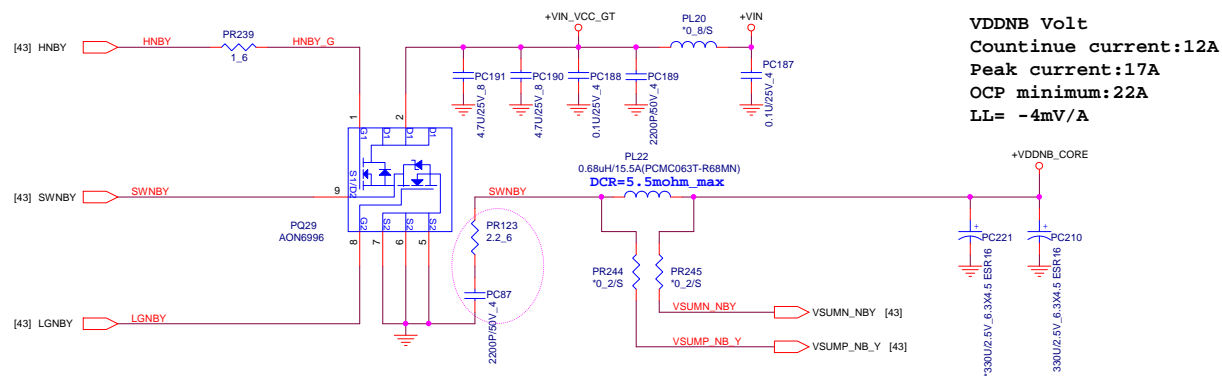
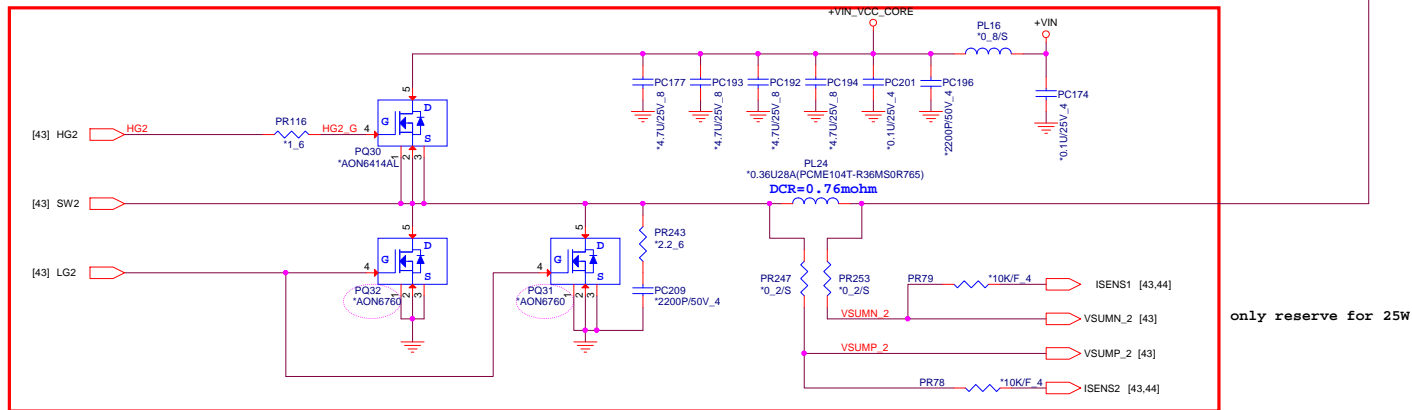
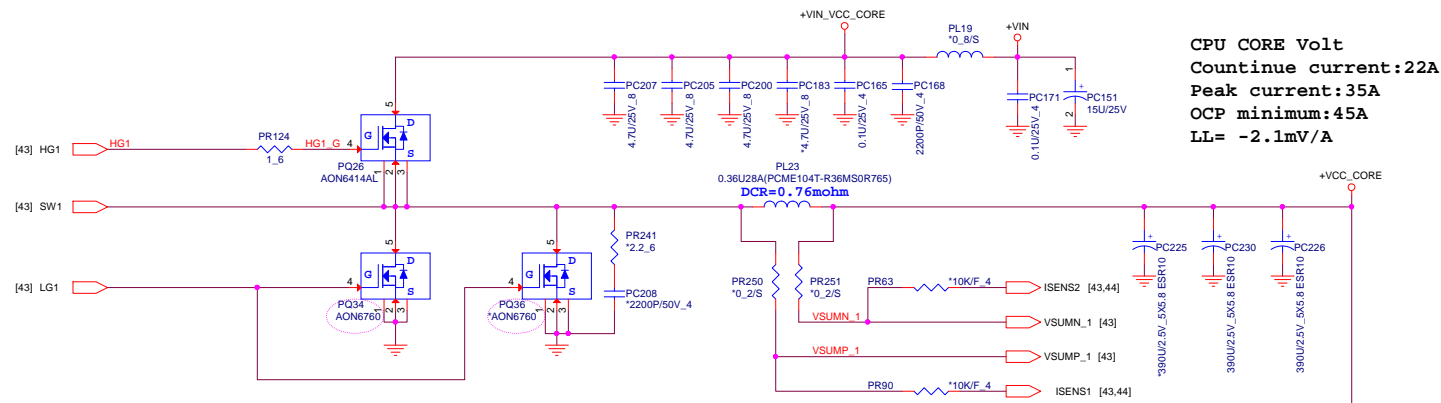
**+0.95V\_DEEP\_SUS +/- 5%**  
**Countinue current:1A**  
**Peak current:2A**

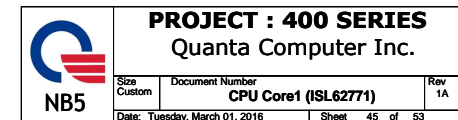


**+0.775V\_DEEP\_SUS +/- 5%**  
**Countinue current:1A**  
**Peak current:2A**

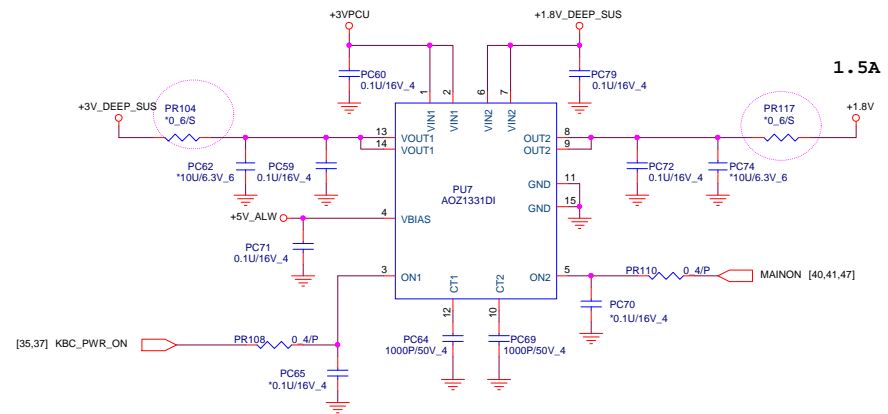
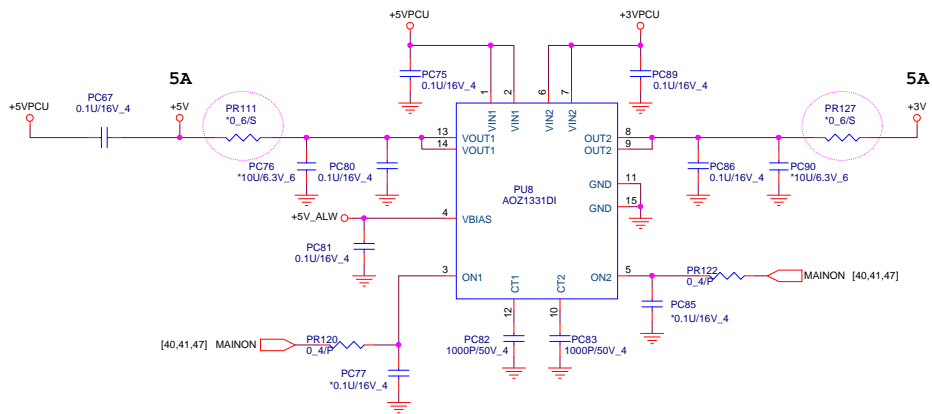






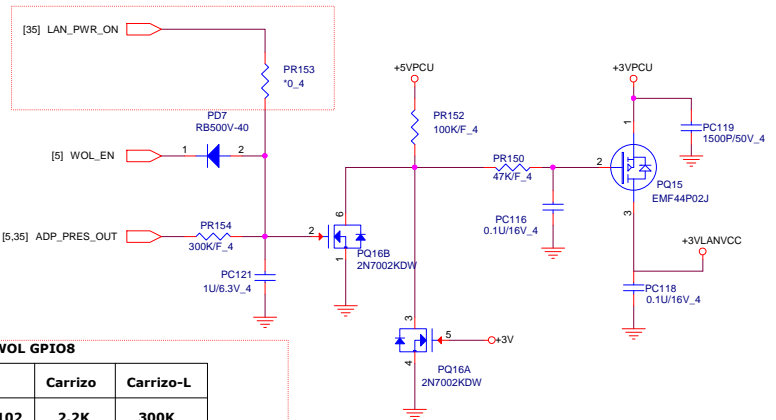






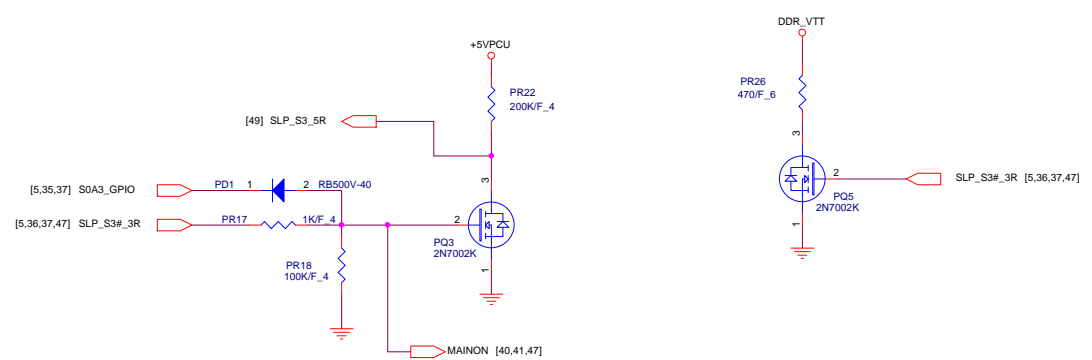
Alfred@DB0, 1103,

1. HP requests to reserve the control the LAN Power from EC Side, so reserved R 0ohm and un-Stuff.



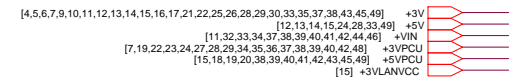
For WOL GPIO8


	Carrizo	Carrizo-L
PR102	2.2K	300K

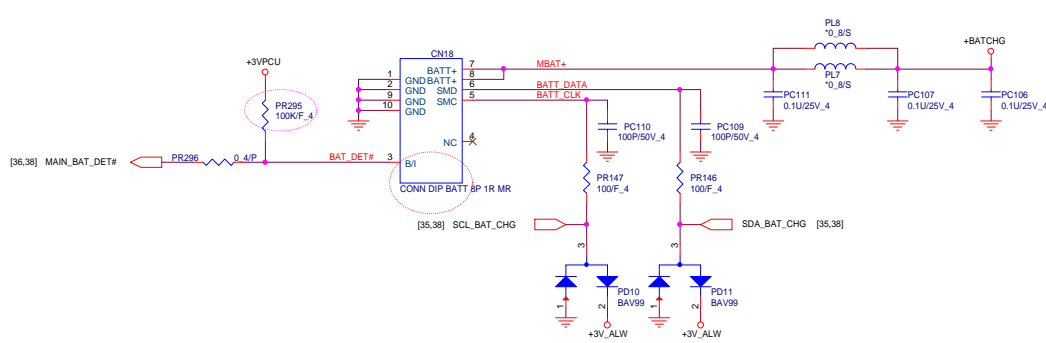
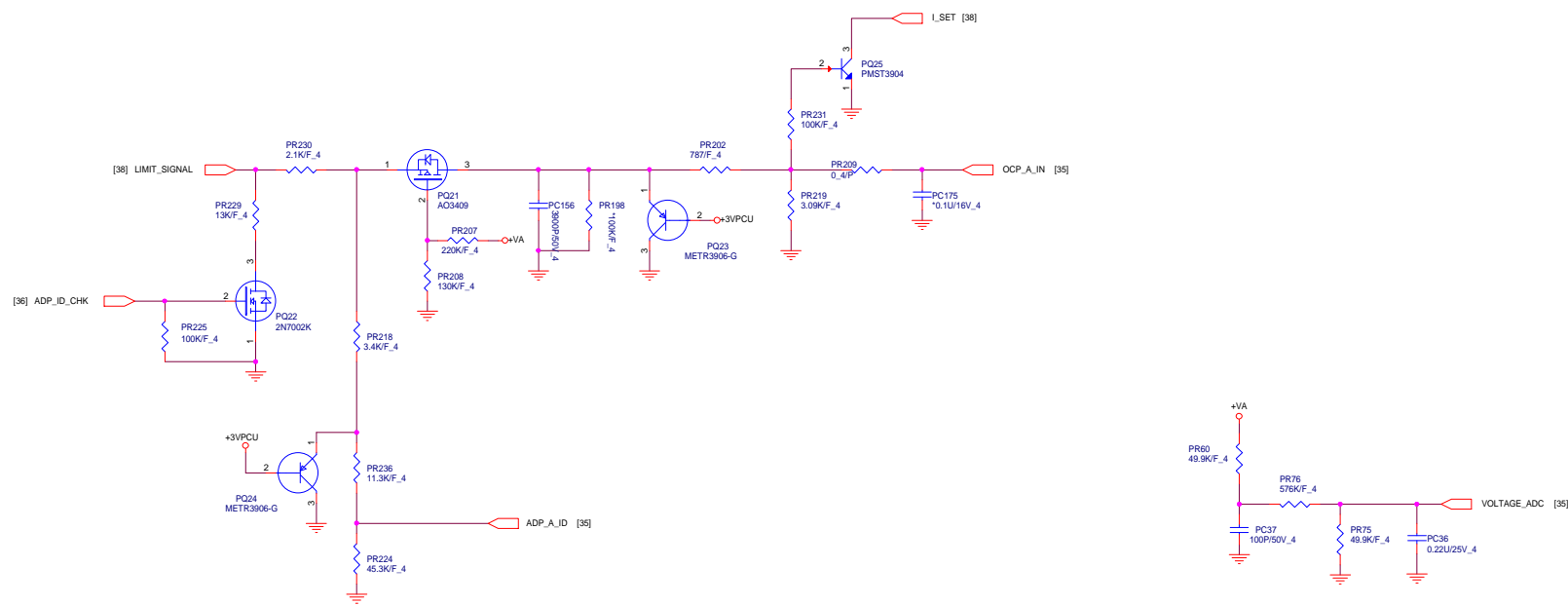


Alfred@DB0, 1103,

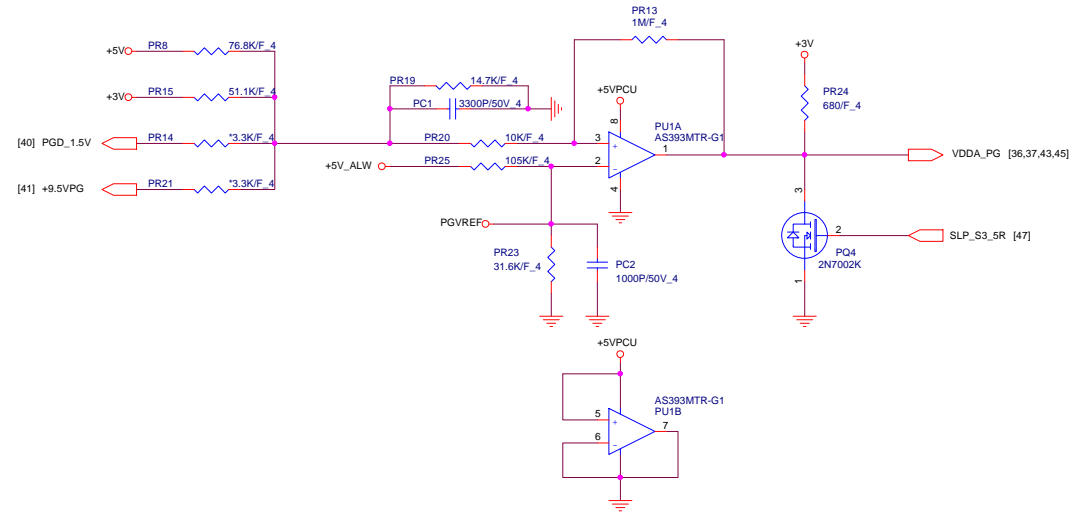
1. Dut to swap the WOL\_EN from AGPIO7 to AGPIO8 and have a PU in EE side, it can use the 300K ohm both BR & ST APU.



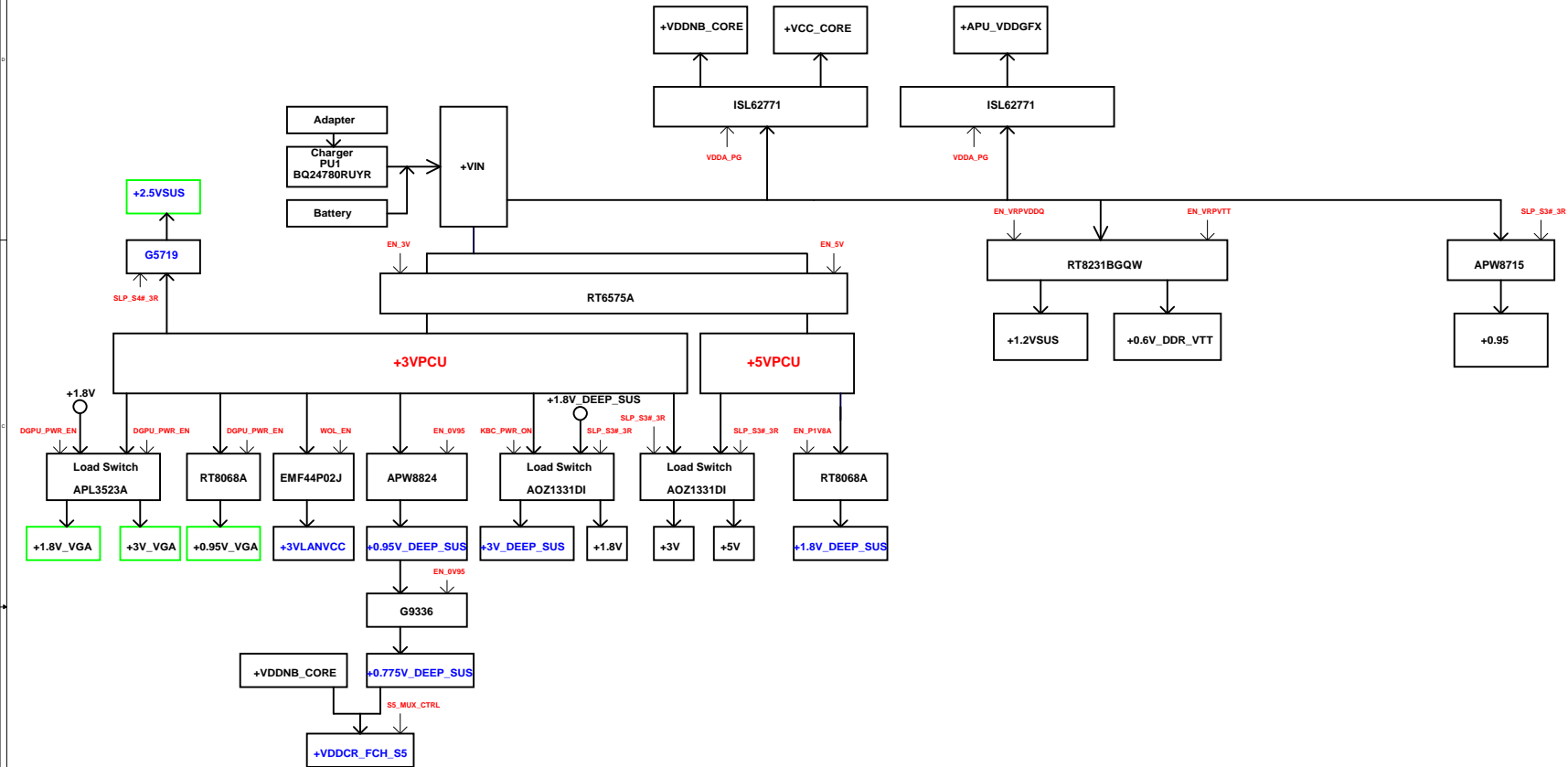
		<b>PROJECT : 400 SERIES</b>	
		Quanta Computer Inc.	
Size Custom	Document Number Dis-charge IC (SLG55448)	Rev 1A	
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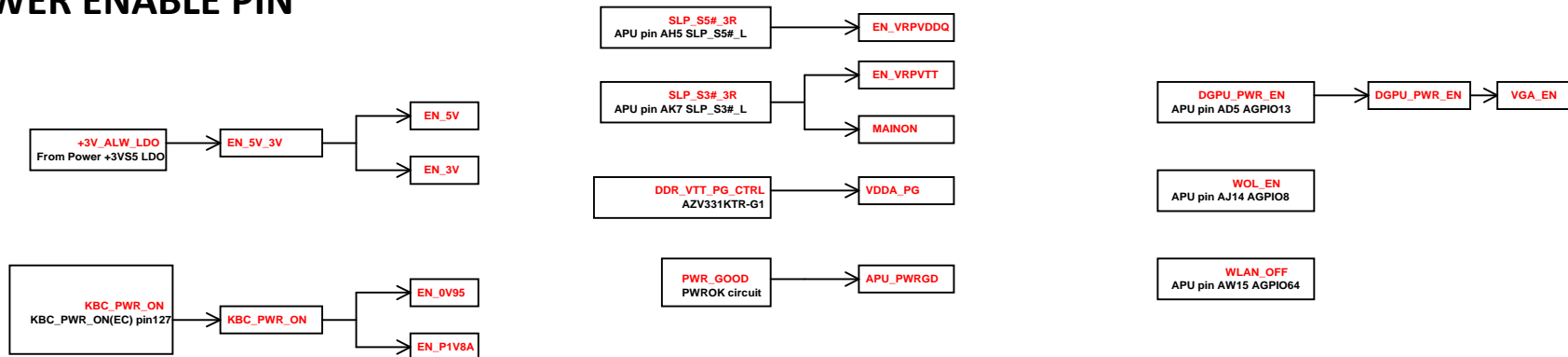




# POWER BLOCK DIAGRAM

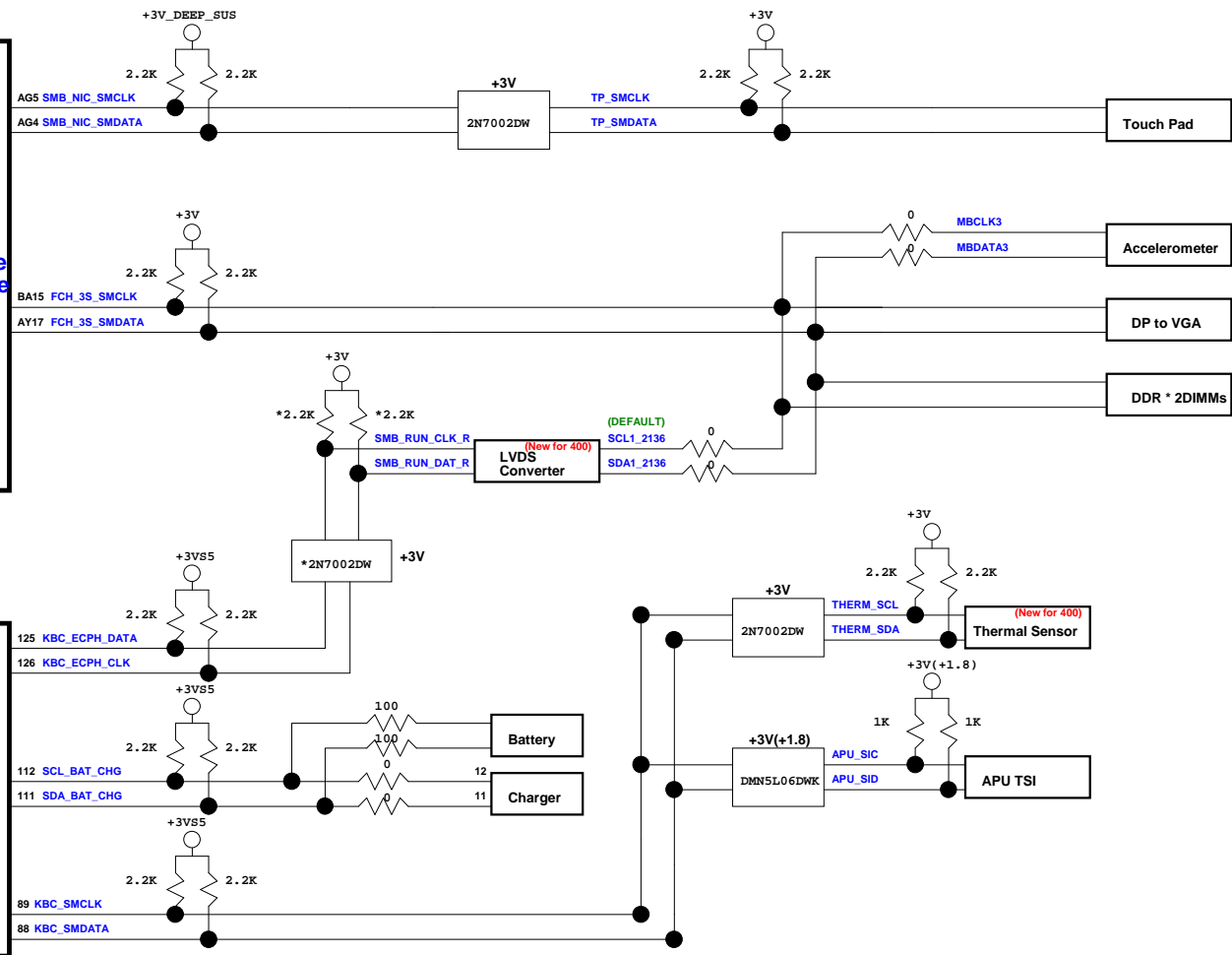


## POWER ENABLE PIN




Bristol Ridge  
Stoney Ridge

EC  
NPCE586H



HSIO Lane	Port Assignment
USB3 #0	NC
USB3 #1	USB Type-C
USB3 #2	USB Type-C
USB3 #3	USB2.0/USB3.0 Combo Jack
PCIE0	NIC
PCIE1	WLAN
PCIE2	NC
PCIE4	Cardreader (PCIE)
DDI0	eDP
DDI1	DP2VGA
DDI2	HDMI
SATA0	HDD/ BOM 0 ohm Option for M.2 SSD
SATA1	ODD
PEG0~3	NC
PEG4~7	NC

USB2.0	Port Assignment
USB2 #0	Camera
USB2 #1	USB2.0(Right side on USB Board)
USB2 #2	USB2.0(Right side on USB Board)
USB2 #3	Bluetooth
USB2 #4	Finger Print
USB2 #5	USB Type-C
USB2 #6	USB Type-C
USB2 #7	USB2.0/USB3.0 Combo Jack

	<b>PROJECT : 400 SERIES</b> <b>Quanta Computer Inc.</b>		
	Size C	Document Number <b>BOM config.</b>	Rev 1A
	Date: Tuesday, March 01, 2016	Sheet	52 of 53

